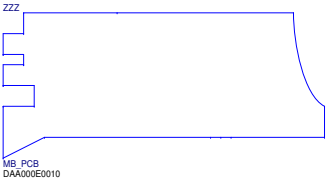


MODEL NAME : CAZ70  
PCB NO : LA-F051P  
BOM P/N : DAA000E0010



# Dell/Compal Confidential

## Schematic Document

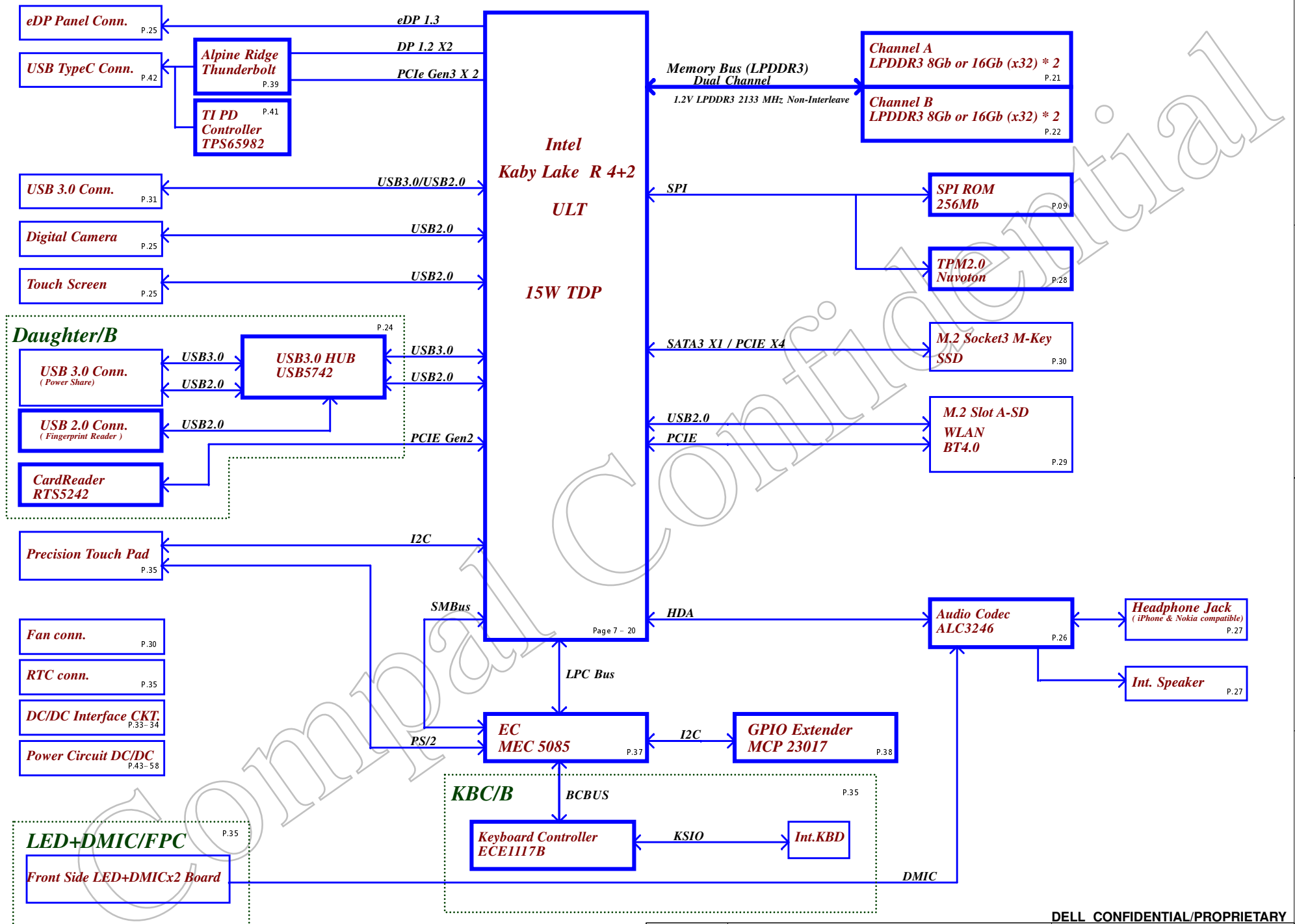
### Dino-R (Kaby Lake ULT)

2017-09-21

Rev: 1.0 (A00)

|     |             |             |             |             |
|-----|-------------|-------------|-------------|-------------|
| CPN | R1          | R3          | R3          | R3          |
|     | DAA000E0010 | DAA000E0011 | DAA000E0012 | DAA000E0013 |

|   |  |                    |  |                               |         |
|---|--|--------------------|--|-------------------------------|---------|
| Security Classification   |  | Compal Secret Data |  | DELL CONFIDENTIAL/PROPRIETARY |         |
| Issued Date   |  | Deciphered Date    |  | Title                         |         |
| 2016/12/16  |  | 2016/12/13         |  | Compal Electronics, Inc.      |         |
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|   |  |                    |  | Document Number               |         |
|   |  |                    |  | LA-F051P                      |         |
| Date: Thursday, September 21, 2017  |  |                    |  | Sheet 1 of 57                 | Rev 0.2 |



# 4+2 CPU Option

PVT 007

UCPU1 SR3LB 4+2@  
SA0009XU1L  
FJ806770328221 SR3LB

UCPU1 SR3LC 4+2@  
SA0009XU1L  
FJ8067703281816 SR3LC



# AR Option

UT1 AR\_SLL42@  
SA0009XU1L  
DSL6340 SLL42 B2

# DRAM Option

# DRAM Config Option

|                       | UD19  | UD20  | UD21  | UD22  |         | MEM_CONFIG0                      | MEM_CONFIG1                      | MEM_CONFIG2                      | MEM_CONFIG3                      | MEM_CONFIG4                      |
|-----------------------|---|---|---|---|---------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| Micron 4G/1866        | <br>SA0009XU1L<br>D3 MT52L256M32D1PF-10707<br>PVT 010 | <br>SA0009XU1L<br>D3 MT52L256M32D1PF-10707<br>PVT 010 | <br>SA0009XU1L<br>D3 MT52L256M32D1PF-10707<br>PVT 010 | <br>SA0009XU1L<br>D3 MT52L256M32D1PF-10707<br>PVT 010 |         | <br>SD028100280<br>10K_0402_5%   | <br>SD028100280<br>10K_0402_5%   | <br>SD028100280<br>10K_0402_5%   | <br>SD028100280<br>10K_0402_5%   | <br>SD028100280<br>10K_0402_5%   |
| Micron 8G/1866        | <br>SA0009XU1L<br>D3 MT52L512M32D2PF-10707<br>PVT 010 | <br>SA0009XU1L<br>D3 MT52L512M32D2PF-10707<br>PVT 010 | <br>SA0009XU1L<br>D3 MT52L512M32D2PF-10707<br>PVT 010 | <br>SA0009XU1L<br>D3 MT52L512M32D2PF-10707<br>PVT 010 |         | <br>SD028100280<br>10K_0402_5%   | <br>SD028100280<br>10K_0402_5%   | <br>SD028100280<br>10K_0402_5%   | <br>SD028100280<br>10K_0402_5%   | <br>SD028100280<br>10K_0402_5%   |
| Hynix 4G/1866         | <br>SA0009XU1L<br>H3CCNNNBGTALAR-NUD                  | <br>SA0009XU1L<br>H3CCNNNBGTALAR-NUD                  | <br>SA0009XU1L<br>H3CCNNNBGTALAR-NUD                  | <br>SA0009XU1L<br>H3CCNNNBGTALAR-NUD                  | PVT 010 | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D |
| Hynix 8G/1866         | <br>SA0009XU1L<br>H3CCNNNBGTALAR-NUD                  | <br>SA0009XU1L<br>H3CCNNNBGTALAR-NUD                  | <br>SA0009XU1L<br>H3CCNNNBGTALAR-NUD                  | <br>SA0009XU1L<br>H3CCNNNBGTALAR-NUD                  |         | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D |
| Samsung 4G/1866       | <br>SA0009XU1L<br>K4E6E304EB-EGCF                     | <br>SA0009XU1L<br>K4E6E304EB-EGCF                     | <br>SA0009XU1L<br>K4E6E304EB-EGCF                     | <br>SA0009XU1L<br>K4E6E304EB-EGCF                     | PVT 015 | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D |
| Samsung 8G/1866       | <br>SA0009XU1L<br>K4E6E304EB-EGCF A311                | <br>SA0009XU1L<br>K4E6E304EB-EGCF A311                | <br>SA0009XU1L<br>K4E6E304EB-EGCF A311                | <br>SA0009XU1L<br>K4E6E304EB-EGCF A311                |         | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D |
| Hynix old die 8G/1866 | <br>SA0009XU1L<br>H3CCNNNBGTALAR-NUD                  | <br>SA0009XU1L<br>H3CCNNNBGTALAR-NUD                  | <br>SA0009XU1L<br>H3CCNNNBGTALAR-NUD                  | <br>SA0009XU1L<br>H3CCNNNBGTALAR-NUD                  | PVT 014 | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D |
| Samsung 16G/2133      | <br>SA0009XU1L<br>K4E6E304EB-EGCF A311                | <br>SA0009XU1L<br>K4E6E304EB-EGCF A311                | <br>SA0009XU1L<br>K4E6E304EB-EGCF A311                | <br>SA0009XU1L<br>K4E6E304EB-EGCF A311                |         | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D |
| Hynix 16G/2133        | <br>SA0009XU1L<br>H3CCNNNBGTALAR-NUD                  | <br>SA0009XU1L<br>H3CCNNNBGTALAR-NUD                  | <br>SA0009XU1L<br>H3CCNNNBGTALAR-NUD                  | <br>SA0009XU1L<br>H3CCNNNBGTALAR-NUD                  |         | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D |
| Micron 16G/2133       | <br>SA0009XU1L<br>MT52L1G32D4PG-093WT-B               | <br>SA0009XU1L<br>MT52L1G32D4PG-093WT-B               | <br>SA0009XU1L<br>MT52L1G32D4PG-093WT-B               | <br>SA0009XU1L<br>MT52L1G32D4PG-093WT-B               |         | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D | <br>SD028100280<br>10K_0402_5%-D |

Board ID Table for AD channel

| RE79 | CE54  | REV |
|------|-------|-----|
| 4.3K | 4700p | TBD |
| 130K | 4700p | TBD |
| 62K  | 4700p | TBD |
| 33K  | 4700p | TBD |
| 8.2K | 4700p | TBD |
| 240K | 4700p | A00 |
| 2.2K | 4700p | X01 |
| 1K   | 4700p | X00 |

PVT 012

BOARD\_ID rise time is measured from 5% to 68%

SMBUS Control Table


|                             | SOURCE  | 23017 | BATTERY | Charger | PD | 5085 | XDP | Audio | Touch Pad |
|-----------------------------|---------|-------|---------|---------|----|------|-----|-------|-----------|
| I2C1A_CLK<br>I2C1A_DATA     | MEC5085 | V     |         |         |    |      |     |       |           |
| I2C1C_CLK<br>I2C1C_DATA     | MEC5085 |       | V       |         |    |      |     |       |           |
| I2C1G_CLK<br>I2C1G_DATA     | MEC5085 |       |         | V       |    |      |     |       |           |
| I2C2A_CLK<br>I2C2A_DATA     | MEC5085 |       |         |         | V  |      |     |       |           |
| PCH_SML0CLK<br>PCH_SML0DATA | PCH     |       |         |         |    |      |     |       |           |
| PCH_SML1CLK<br>PCH_SML1DATA | PCH     |       |         |         |    | V    |     |       |           |
| SMBCLK<br>SMBDATA           | PCH     |       |         |         |    |      | V   |       |           |
| I2C0_CLK<br>I2C0_DATA       | PCH     |       |         |         |    |      |     |       |           |
| I2C1_CLK<br>I2C1_DATA       | PCH     |       |         |         |    |      |     |       | V         |


| CLK | DIFFERENTIAL CLK# | DESTINATION    | PCI EXPRESS PORT# | DESTINATION    |
|-----|-------------------|----------------|-------------------|----------------|
|     | CLKOUT_PCIE0      | Alpine Ridge   | Lane 1            | Alpine Ridge   |
|     | CLKOUT_PCIE1      | NGFF CARD WLAN | Lane 2            | Alpine Ridge   |
|     | CLKOUT_PCIE2      |                | Lane 3            |                |
|     | CLKOUT_PCIE3      | M.2 SSD / PCIe | Lane 4            |                |
|     | CLKOUT_PCIE4      |                | Lane 5            | NGFF CARD WLAN |
|     | CLKOUT_PCIE5      | Card Reader    | Lane 6            | Card Reader    |
|     | FLEX CLK#         | DESTINATION    | Lane 7            |                |
|     | CLKOUT_LPC_0      | EC LPC         | Lane 8            |                |
|     | CLKOUT_LPC_1      | Debug          | Lane 9            | M.2 SSD        |
|     |                   |                | Lane 10           | M.2 SSD        |
|     |                   |                | Lane 11           | M.2 SSD        |
|     |                   |                | Lane 12 / SATA 2  | M.2 SSD        |

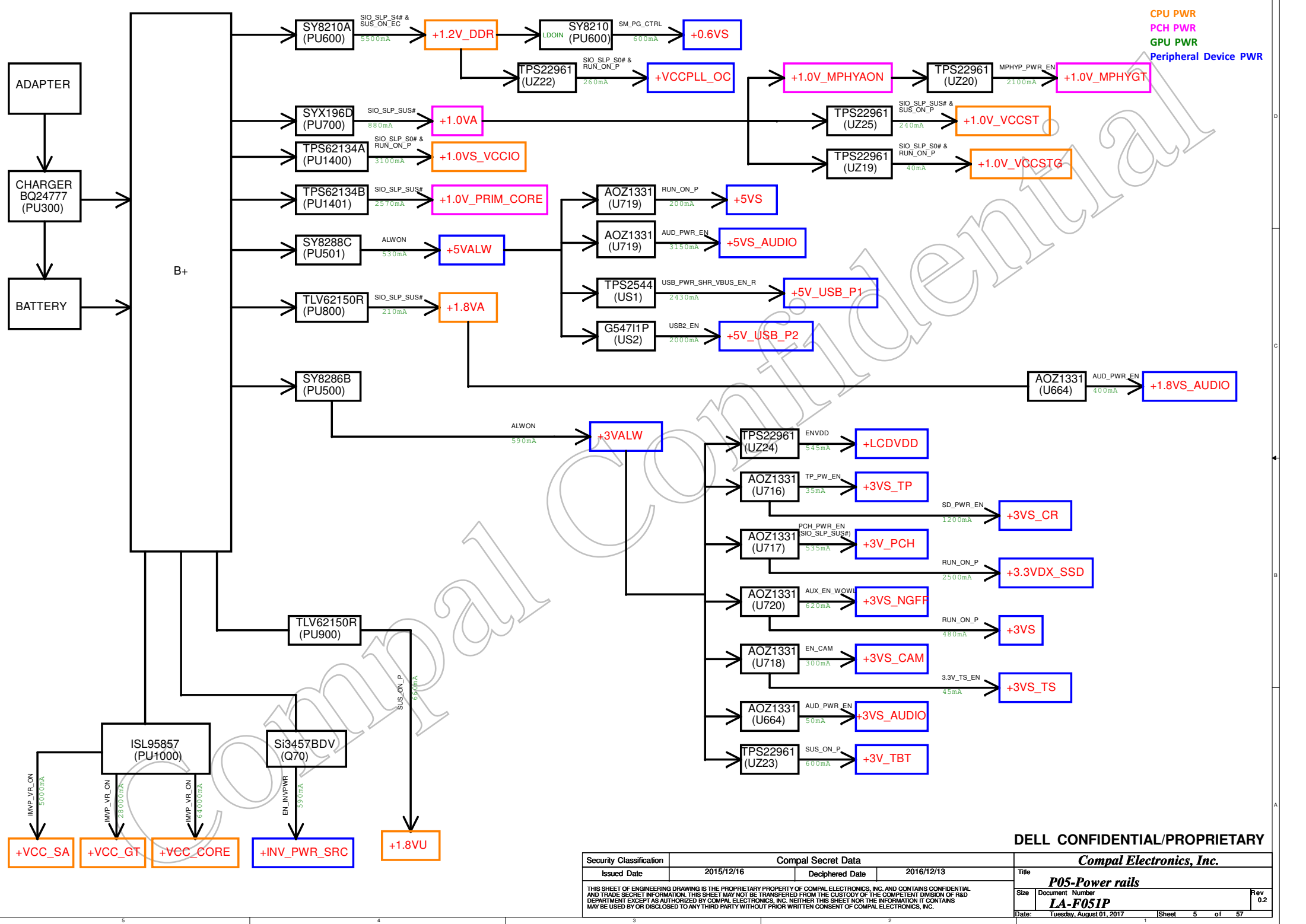
| PCH<br>USB 2.0<br>Port<br>Mapping | USB PORT# | DESTINATION           |
|-----------------------------------|-----------|-----------------------|
|                                   | 1         | External USB3(On IOB) |
|                                   | 2         | External USB3(On MB)  |
|                                   | 3         | NGFF CARD WLAN        |
|                                   | 4         | Touch Panel           |
|                                   | 5         | Camera                |
|                                   | 6         |                       |
|                                   | 7         |                       |
|                                   |           |                       |
|                                   |           |                       |
| PCH<br>USB 3.0<br>Port<br>Mapping | 1         | External USB3(On IOB) |
|                                   | 2         | External USB3(On MB)  |
|                                   |           |                       |
| PCH<br>DDI<br>Port<br>Mapping     | DDI PORT# | DESTINATION           |
|                                   | 1         | Alpine Ridge          |
|                                   | 2         | Alpine Ridge          |
|                                   |           |                       |

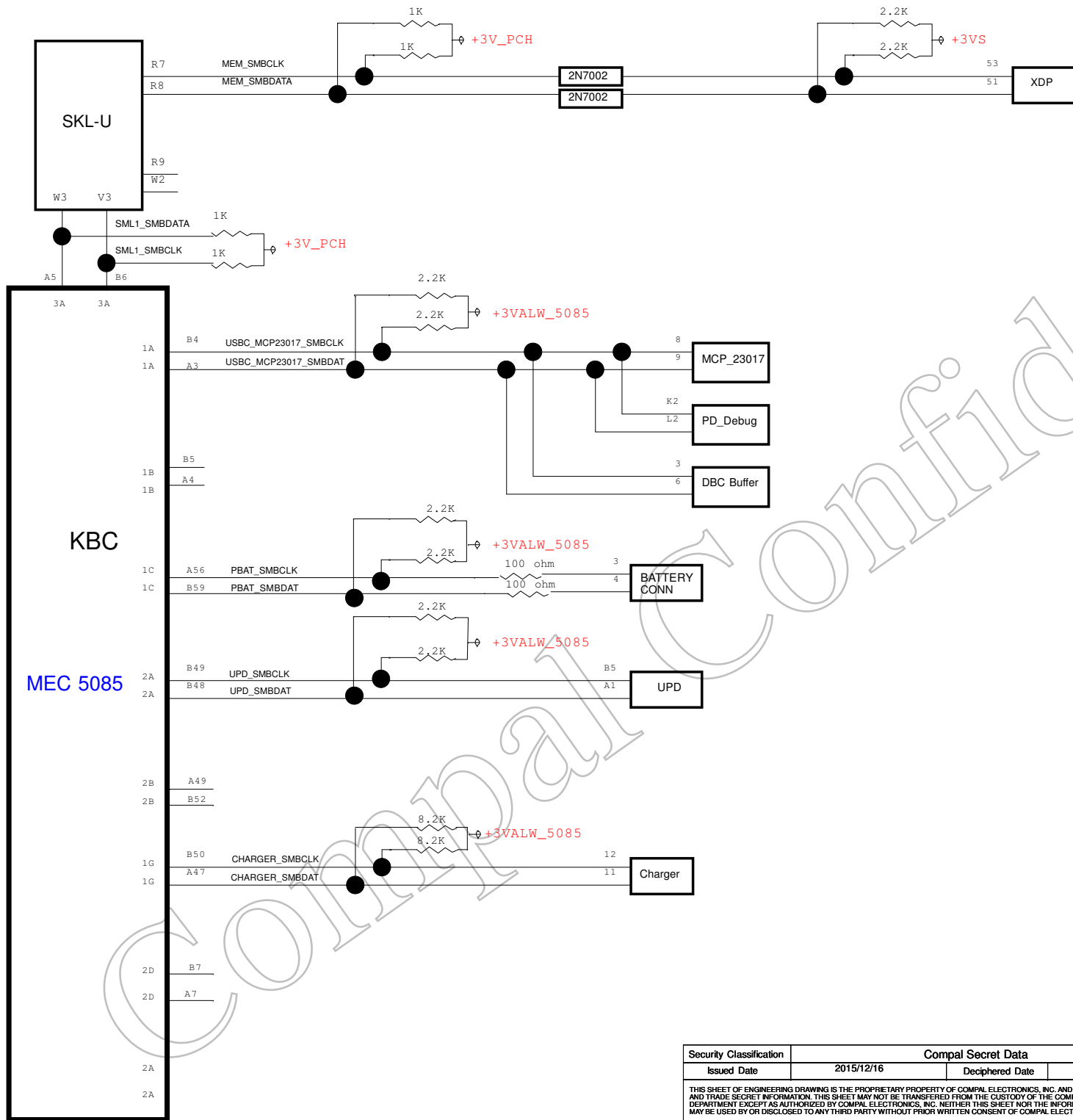
| SATA PORT# | DESTINATION |
|------------|-------------|
| SATA-0     |             |
| SATA-1A    |             |
| SATA-1B    |             |
| SATA-2     | M.2 SSD     |
|            |             |
|            |             |

Symbol Note :

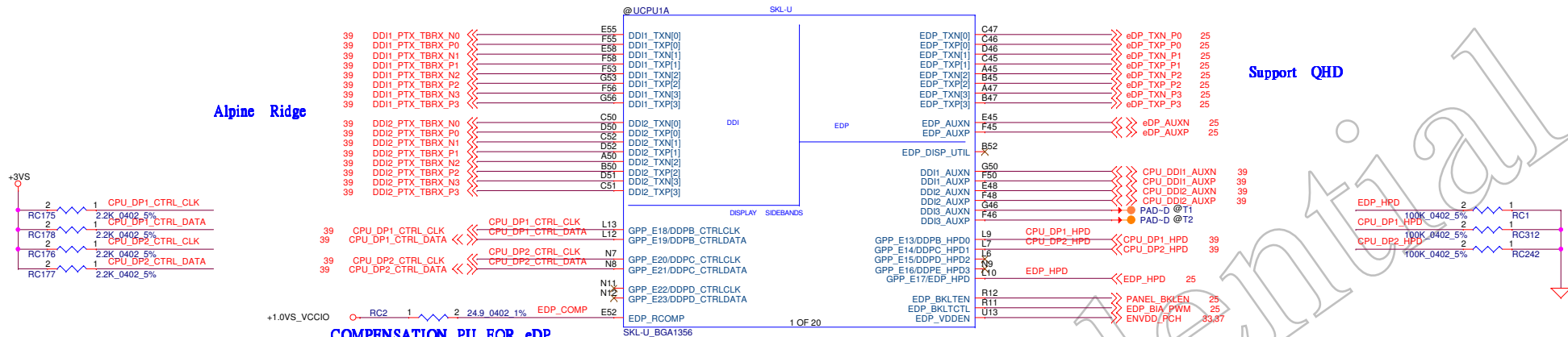
 : means Digital Ground

 : means Analog Ground





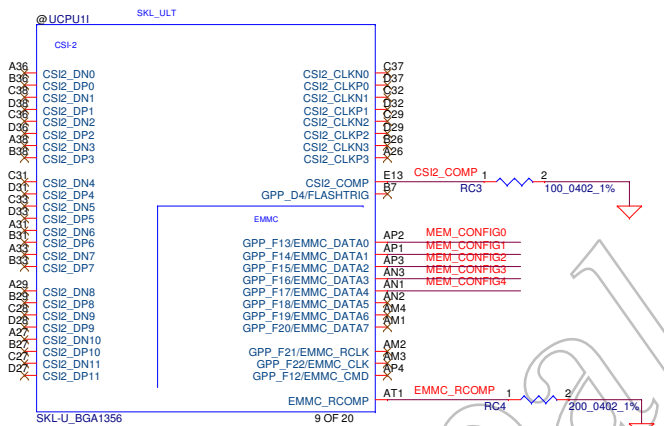
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|   |  |  |  | Document Number                |  |  |  | LA-F051P                      |  |  |  |
|   |  |  |  | Rev                            |  |  |  | 0.2                           |  |  |  |
|   |  |  |  | Date: Tuesday, August 01, 2017 |  |  |  | Sheet 6 of 57                 |  |  |  |



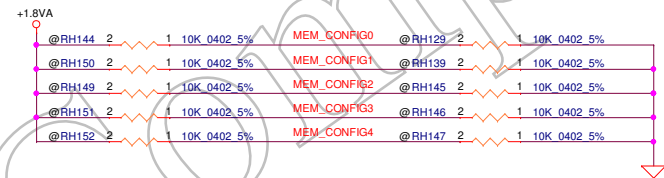
### COMPENSATION PU FOR eDP

CAD Note: Trace width=5 mils, Isolation Spacing=25mil,  
Max length=600 mils.

SKL-U Ballout Rev0.71 & INTEL symbol Rev1.0



### DDR Memory Configuration Type Strap pin



| GPIO Pin | Pin Name    | Micron 4G | Micron 8G | Micron 16G | Hynix 4G | Hynix 8G | Hynix 16G | Samsung 1866/4G | Samsung 1866/8G | Samsung 1866/16G |
|----------|-------------|-----------|-----------|------------|----------|----------|-----------|-----------------|-----------------|------------------|
| GPP_F13  | MEM_CONFIG0 | 0         | 1         | 0          | 1        | 0        | 1         | 0               | 1               | 0                |
| GPP_F14  | MEM_CONFIG1 | 0         | 0         | 1          | 1        | 0        | 0         | 1               | 1               | 0                |
| GPP_F15  | MEM_CONFIG2 | 0         | 0         | 0          | 0        | 1        | 1         | 1               | 1               | 0                |
| GPP_F16  | MEM_CONFIG3 | 0         | 0         | 0          | 0        | 0        | 0         | 0               | 0               | 1                |
| GPP_F17  | MEM_CONFIG4 | 0         | 0         | 0          | 0        | 0        | 0         | 0               | 0               | 0                |

| GPIO Pin | Pin Name    | Micron 4G | Micron 8G | Micron 16G | Hynix 4G | Hynix 8G | Hynix 16G | New Hynix 4G | New Hynix 8G | New Hynix 16G |
|----------|-------------|-----------|-----------|------------|----------|----------|-----------|--------------|--------------|---------------|
| GPP_F13  | MEM_CONFIG0 | 1         | 0         | 1          | 0        | 1        | 0         | 1            | 0            | 1             |
| GPP_F14  | MEM_CONFIG1 | 0         | 1         | 1          | 0        | 0        | 1         | 1            | 0            | 0             |
| GPP_F15  | MEM_CONFIG2 | 0         | 0         | 0          | 1        | 1        | 1         | 1            | 0            | 0             |
| GPP_F16  | MEM_CONFIG3 | 1         | 1         | 1          | 1        | 1        | 1         | 1            | 0            | 0             |
| GPP_F17  | MEM_CONFIG4 | 0         | 0         | 0          | 0        | 0        | 0         | 0            | 1            | 1             |

| GPIO Pin | Pin Name    | Micron 4G | Micron 8G | Micron 16G | Hynix 4G | Hynix 8G | Hynix 16G | Samsung 4G | Samsung 8G | Samsung 16G |
|----------|-------------|-----------|-----------|------------|----------|----------|-----------|------------|------------|-------------|
| GPP_F13  | MEM_CONFIG0 | 0         | 1         | 0          | 1        | 0        | 1         | 0          | 1          | 0           |
| GPP_F14  | MEM_CONFIG1 | 1         | 1         | 0          | 0        | 1        | 1         | 0          | 0          | 1           |
| GPP_F15  | MEM_CONFIG2 | 0         | 0         | 1          | 1        | 1        | 1         | 0          | 0          | 0           |
| GPP_F16  | MEM_CONFIG3 | 0         | 0         | 0          | 0        | 0        | 0         | 1          | 1          | 1           |
| GPP_F17  | MEM_CONFIG4 | 1         | 1         | 1          | 1        | 1        | 1         | 1          | 1          | 1           |

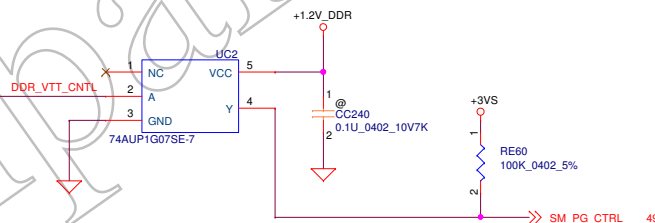
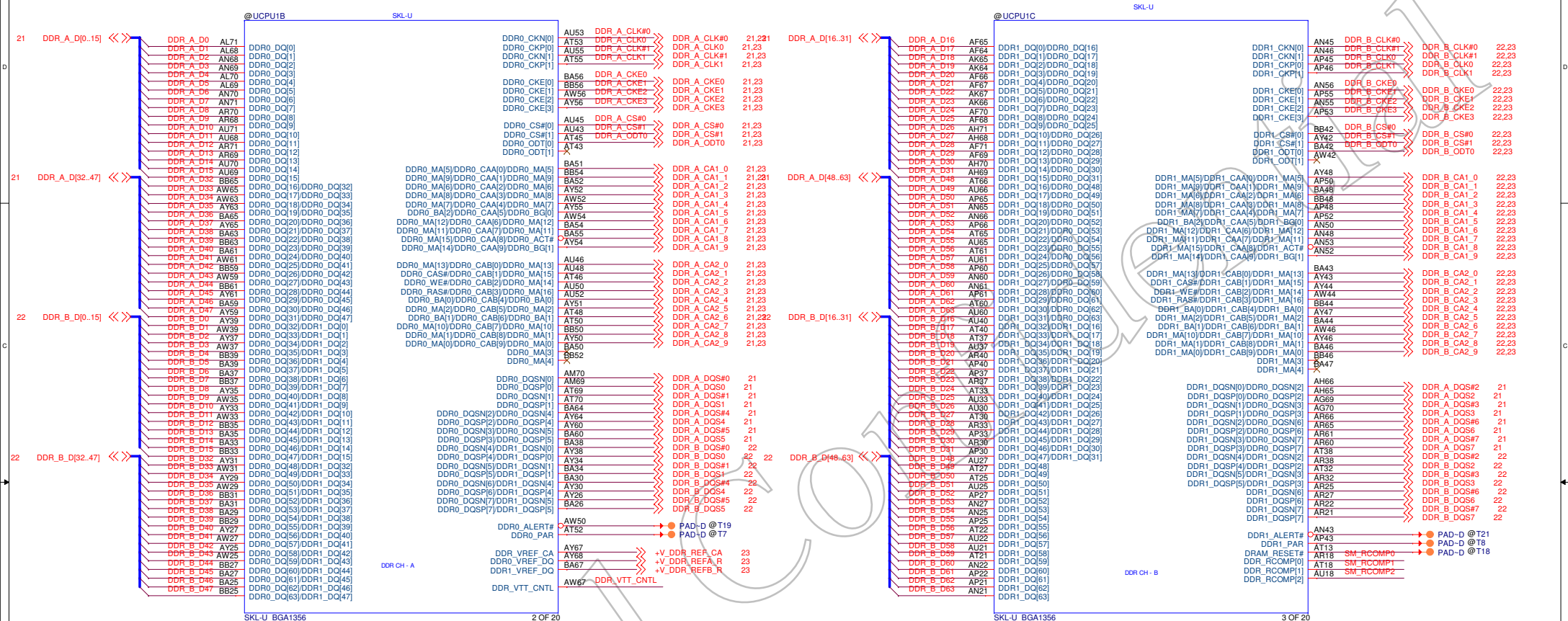
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| Security Classification   | Compal Secret Data |                 | Title      |   |
|---|--------------------|-----------------|------------|---|
| Issued Date   | 2015/12/16         | Deciphered Date | 2016/12/13 |   |
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| Date: Tuesday, August 01, 2017  |                    |                 |            | Sheet 7 of 57                               |



# LPDDR3, Ballout for side by side(Non-Interleave)



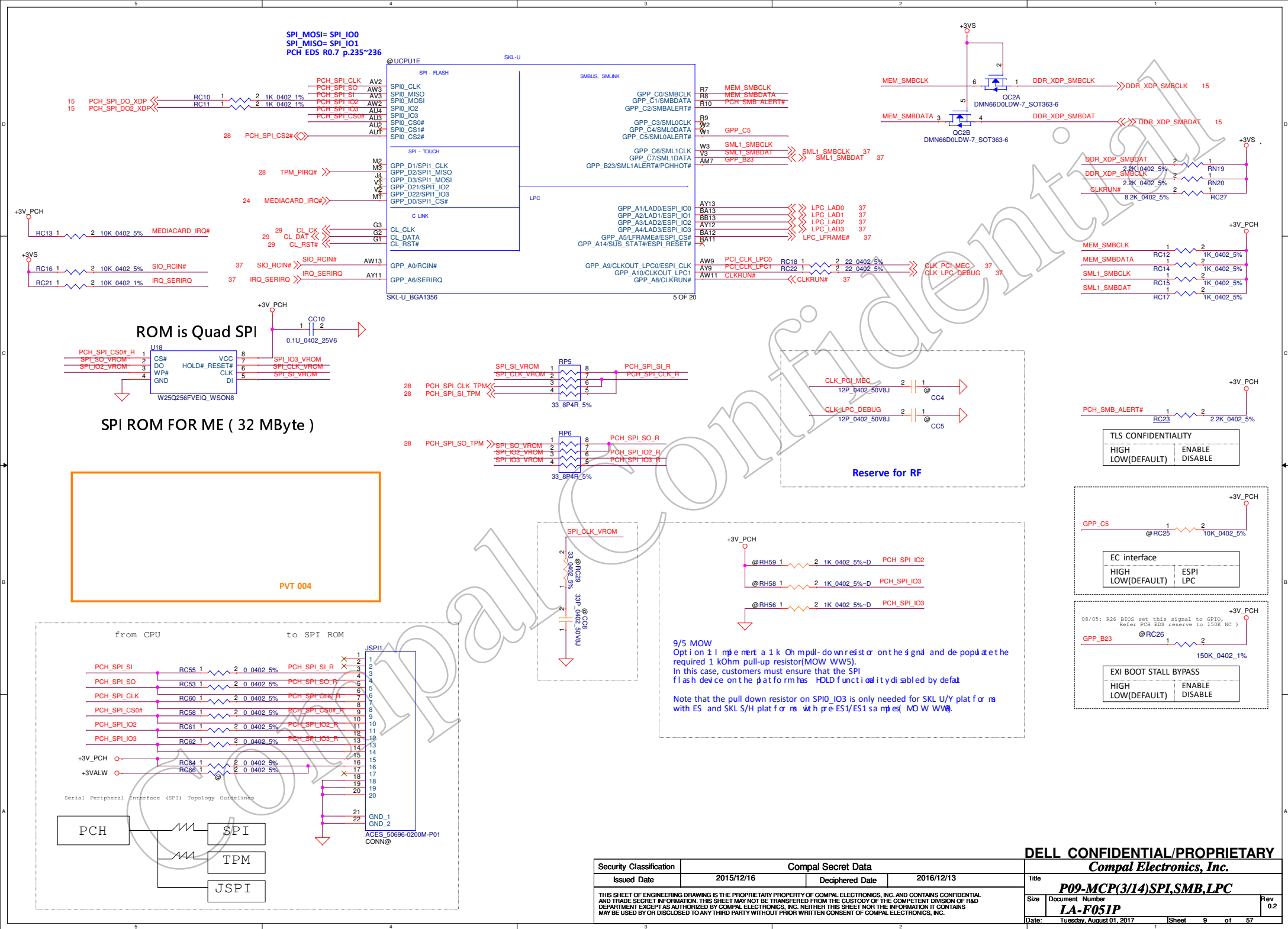
## LPDDR3 COMPENSATION SIGNALS

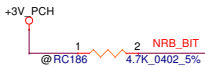
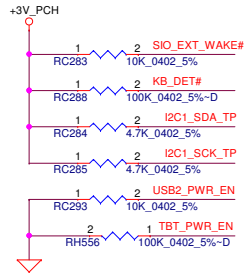
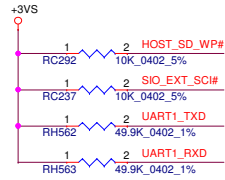


CAD Note:  
Trace width=12~15 mil, Spacing=20 mils  
Max trace length= 500 mil

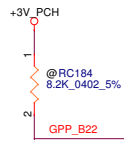
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| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc. |                          |
| Issued Date   | 2015/12/16 | Deciphered Date    | 2016/12/13 | Title                    | P08-MCP(2/14)LPDDR3      |
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|   |            |                    |            | Date:                    | Tuesday, August 01, 2017 |
|   |            |                    |            | Sheet                    | 8 of 57                  |
|   |            |                    |            | Rev                      | 0.2                      |



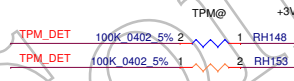
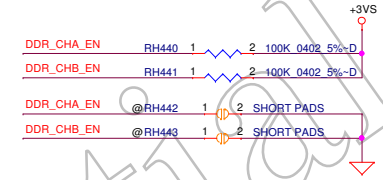
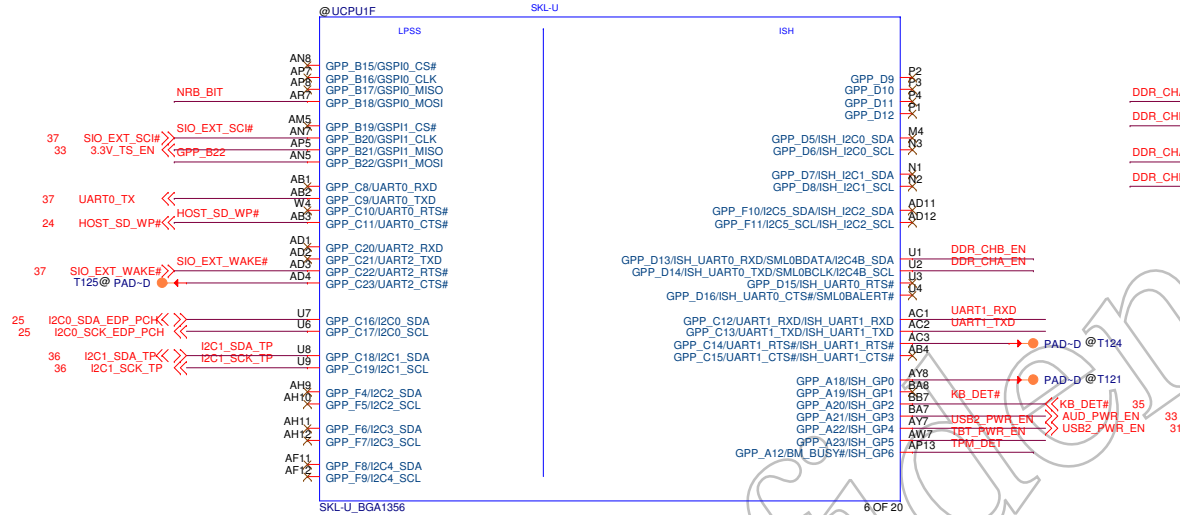




| NO REBOOT STRAP      |                            |
|----------------------|----------------------------|
| HIGH<br>LOW(DEFAULT) | No REBOOT<br>REBOOT ENABLE |
| Weak IPD             |                            |

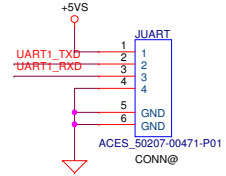


| BOOT BIOS Destination |            |
|-----------------------|------------|
| HIGH<br>LOW(DEFAULT)  | LPC<br>SPI |



### TPM BOM Optional

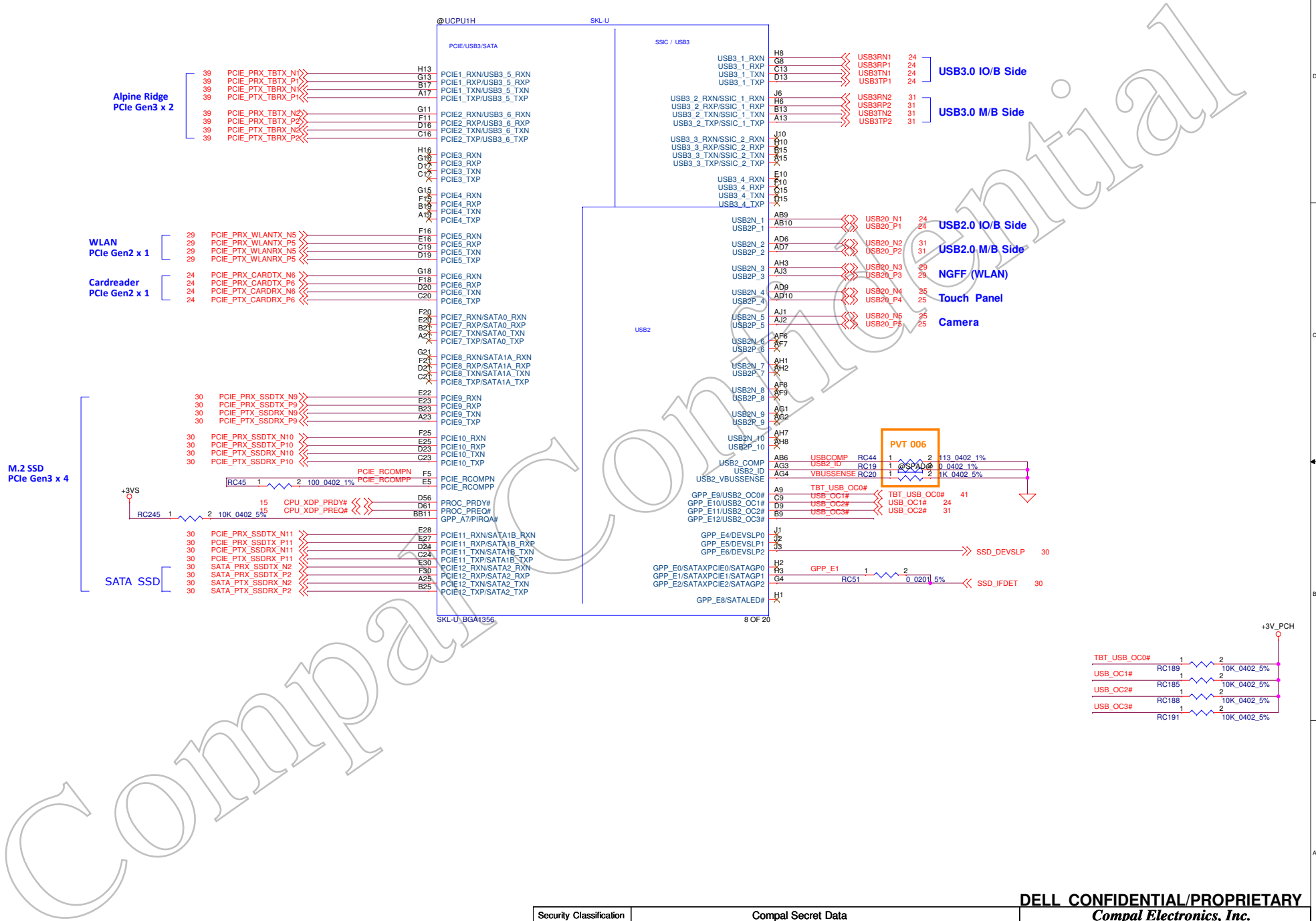
| TPM DET |                          |
|---------|--------------------------|
| TPM     | 1 = W/TPM<br>0 = W/O TPM |



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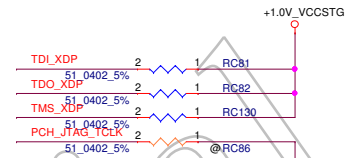
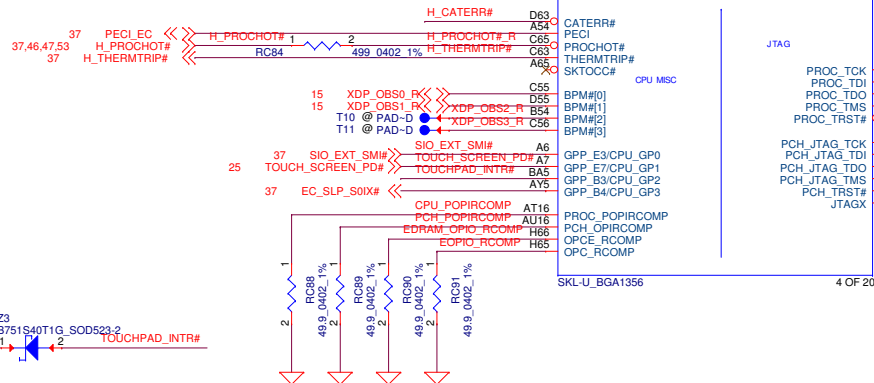
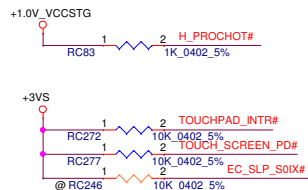
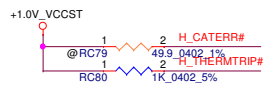
Compal Electronics, Inc.

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|---|------------|--------------------|------------|--------------------------------|--------------------------|
| Issued Date   | 2015/12/16 | Deciphered Date    | 2016/12/13 | P10-MCP(4/14)GSPI,I2C,UART,ISH |                          |
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|   |            |                    |            | Sheet                          | 10 of 57                 |

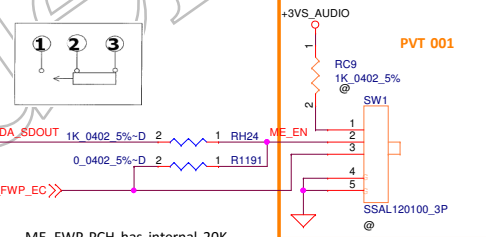


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|                         |  |  |  |                    |                 |                               | Compal Electronics, Inc.       |
|                         |  |  |  |                    |                 |                               | P11-MCP(5/14)PCIE,USB,SATA     |
|                         |  |  |  |                    |                 |                               | Size Document Number           |
|                         |  |  |  |                    |                 |                               | LA-F051P                       |
|                         |  |  |  |                    |                 |                               | Rev 0.2                        |
|                         |  |  |  |                    |                 |                               | Date: Tuesday, August 01, 2017 |
|                         |  |  |  |                    |                 |                               | Sheet 11 of 57                 |





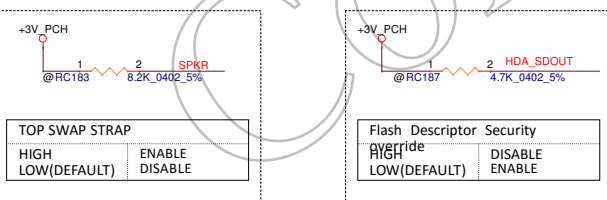
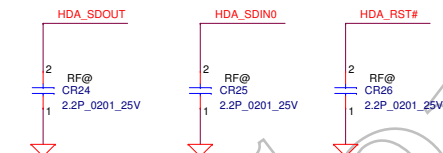
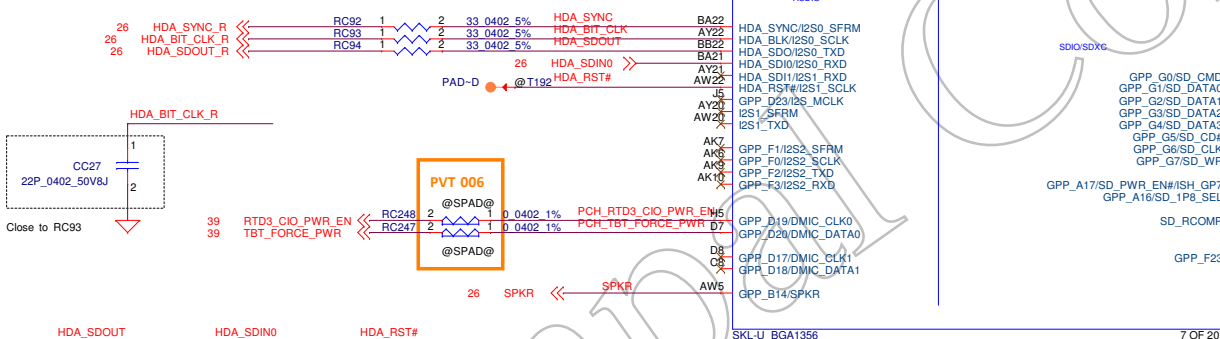
Service Mode Switch:  
Add a switch to ME\_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FRT.



ME\_FWP\_PCH has internal 20K

FLASH DESCRIPTOR SECURITY OVERRIDE

Disable ME Protect (ME can be updated) ----> Pin1 & Pin2 short  
Enable ME Protect (ME cannot be updated)-->Pin3 & Pin2 short(Default position)



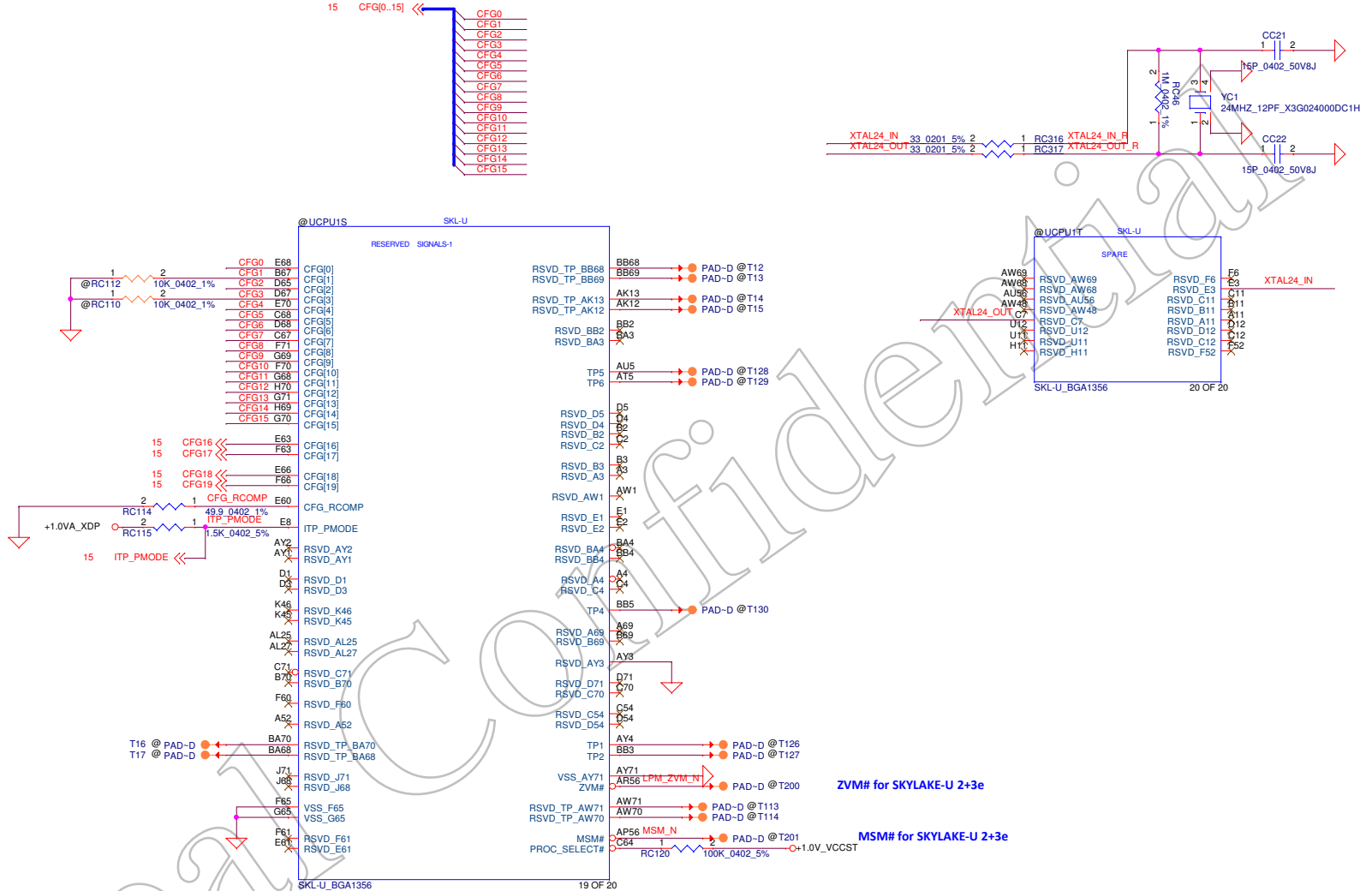
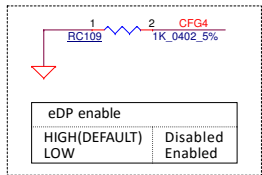
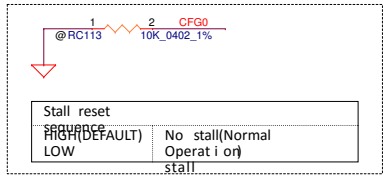
TOP SWAP STRAP

|              |         |
|--------------|---------|
| HIGH         | ENABLE  |
| LOW(DEFAULT) | DISABLE |

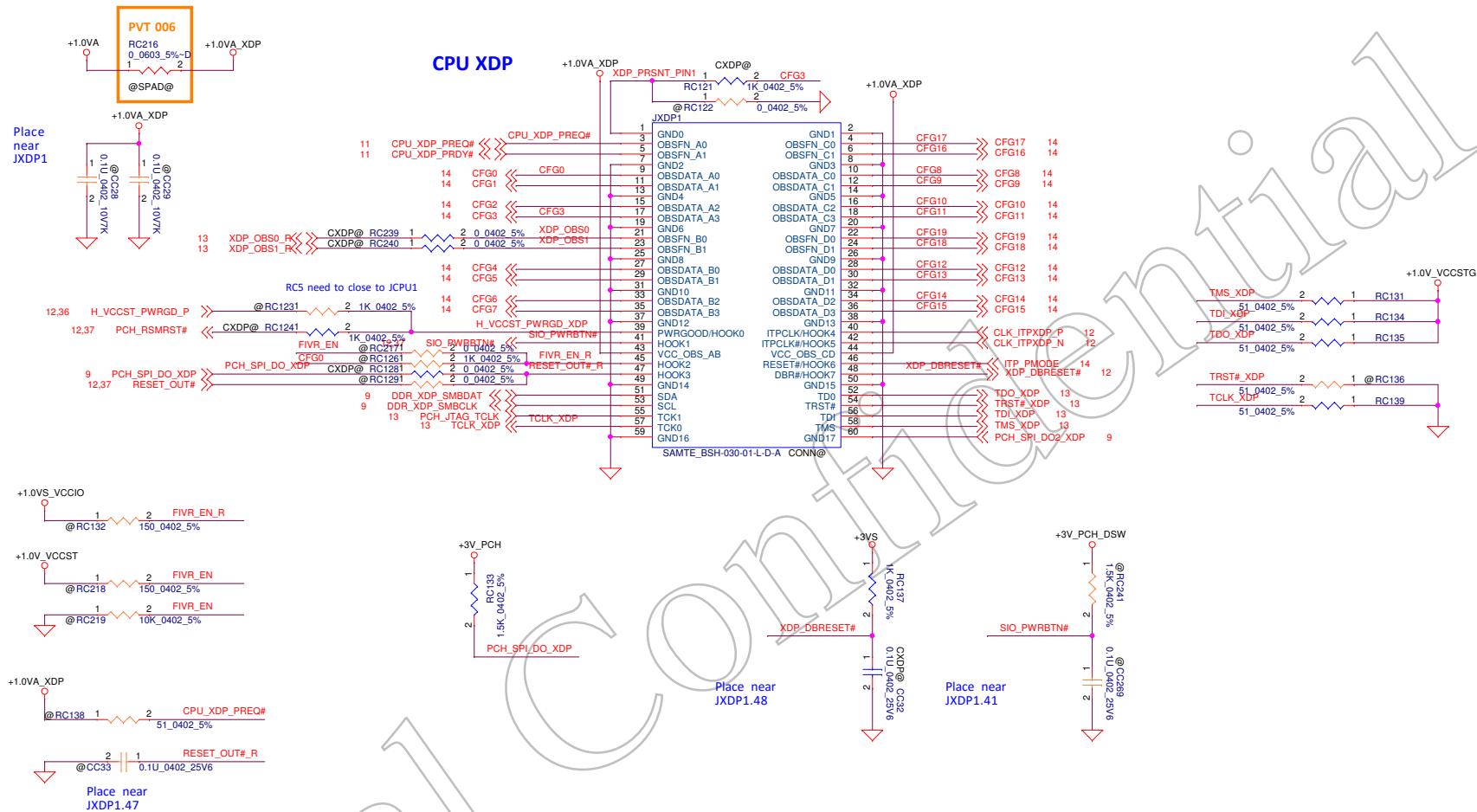
Flash Descriptor Security

|              |         |
|--------------|---------|
| HIGH         | DISABLE |
| LOW(DEFAULT) | ENABLE  |

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|   |            |                    |            | Size                          | Document Number                 |
|   |            |                    |            | LA-F051P                      |                                 |
|   |            |                    |            | Rev                           | 0.2                             |
|   |            |                    |            | Date                          | Tuesday, August 01, 2017        |
|   |            |                    |            | Sheet                         | 13 of 57                        |





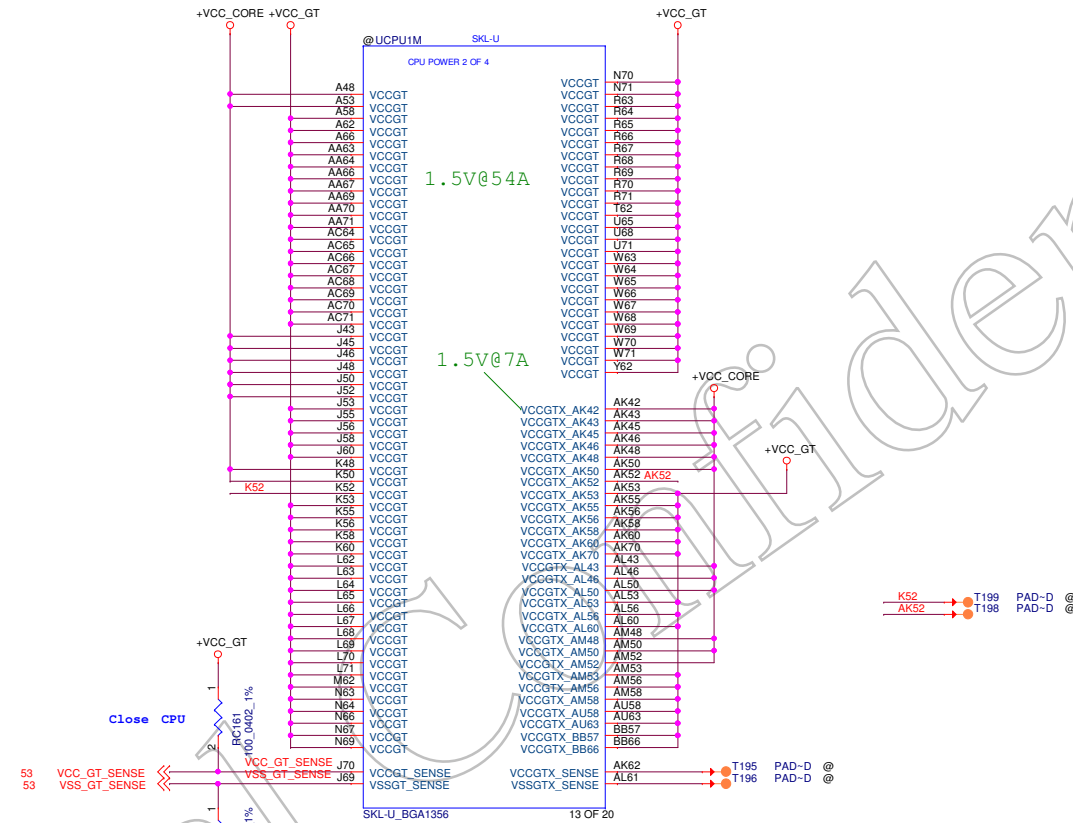


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|   |  |  |  | LA-F051P           |  |  |  | Rev                            |  |  |  |
|   |  |  |  | 0.2                |  |  |  | Date: Tuesday, August 01, 2017 |  |  |  |
|   |  |  |  | Sheet 15 of 57     |  |  |  |                                |  |  |  |





+VCCGT: 0.55~1.5V, 28A



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2016/12/13

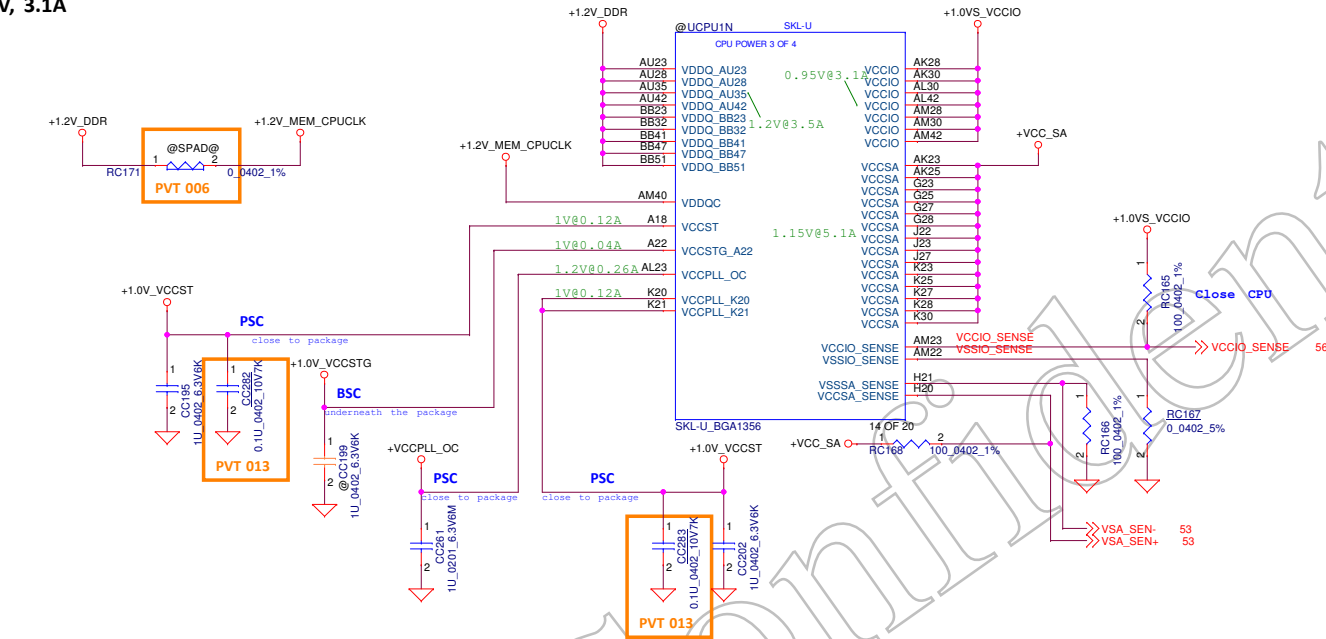
Title  
P17-MCP(11/14)PWR-VCCGT

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Document Number  
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Rev  
0.2

Date  
Tuesday, August 01, 2017  
Sheet  
17 of 57

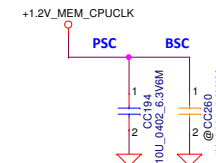
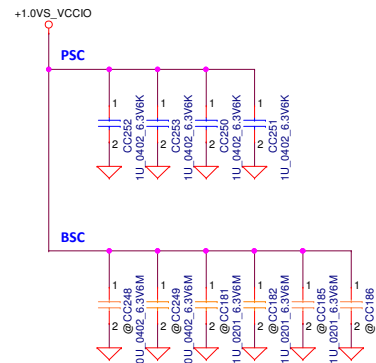
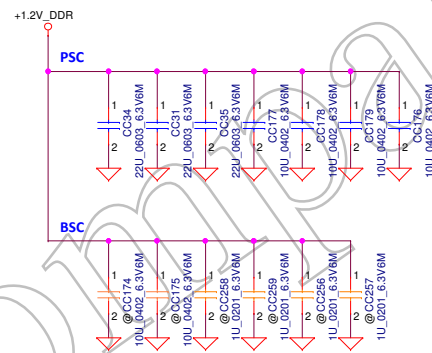
+1.2V\_DDR: 1.2V, 3.5A  
 +1.0V\_VCCST: 1V, 120mA; VCCPLL: 1V, 120mA  
 +1.0V\_VCCSTG: 1V, 40mA  
 +VCCPLL\_OC: 1.2V, 260mA  
 +1.0VS\_VCCIO: 0.85~0.95V, 3.1A  
 +VCC\_SA: 1.15V, 5.0A



+1.2V\_DDR Decoupling Requirement  
 Back Side (underneath the package):  
 100U\_0402\*2 pcs + 1U\_0201\*4 pcs (8)  
 Primary Side (close to package):  
 100U\_0402\*4 pcs + 22U\_0603\*3 pcs

+1.0VS\_VCCIO Decoupling Requirement  
 Back Side (underneath the package):  
 100U\_0402\*2 pcs + 1U\_0201\*4 pcs (8)  
 Primary Side (close to package):  
 10U\_0402\*4 pcs

+1.2V\_MEM\_CPUCLK (VDDQ) Place on CPU  
 Back Side (underneath the package):  
 1U\_0201\*1 pcs (8)  
 Primary Side (close to package):  
 100U\_0402 \* 1 pcs

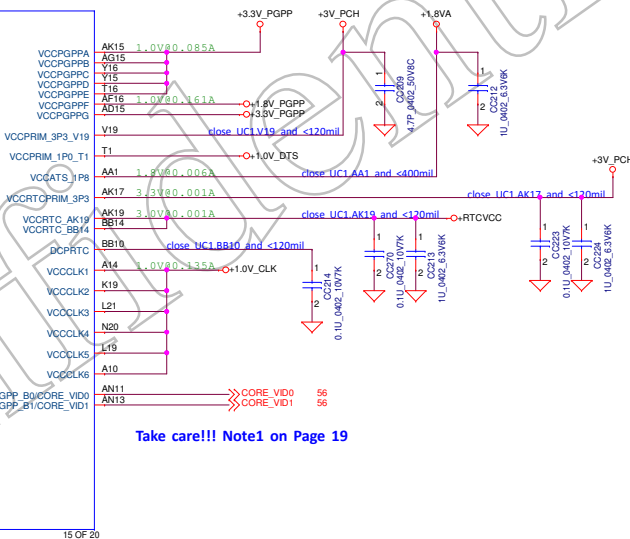
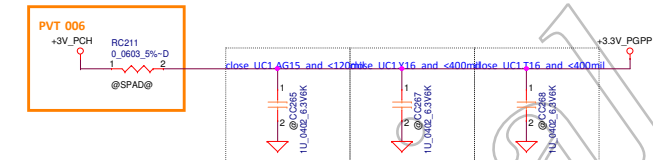
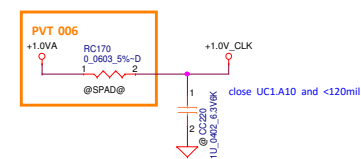
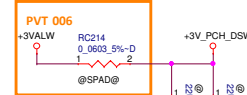
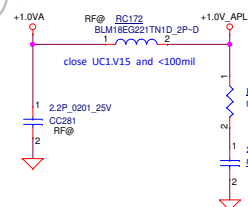
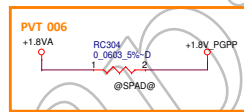
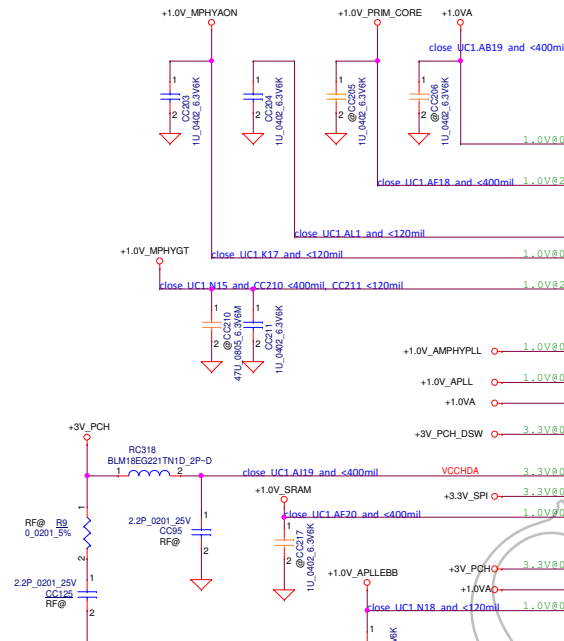
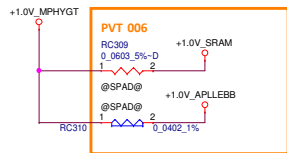
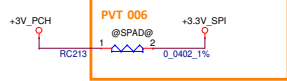
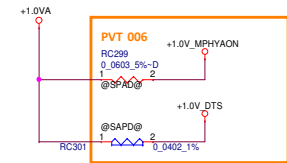
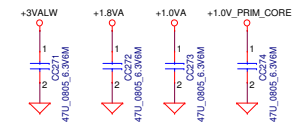


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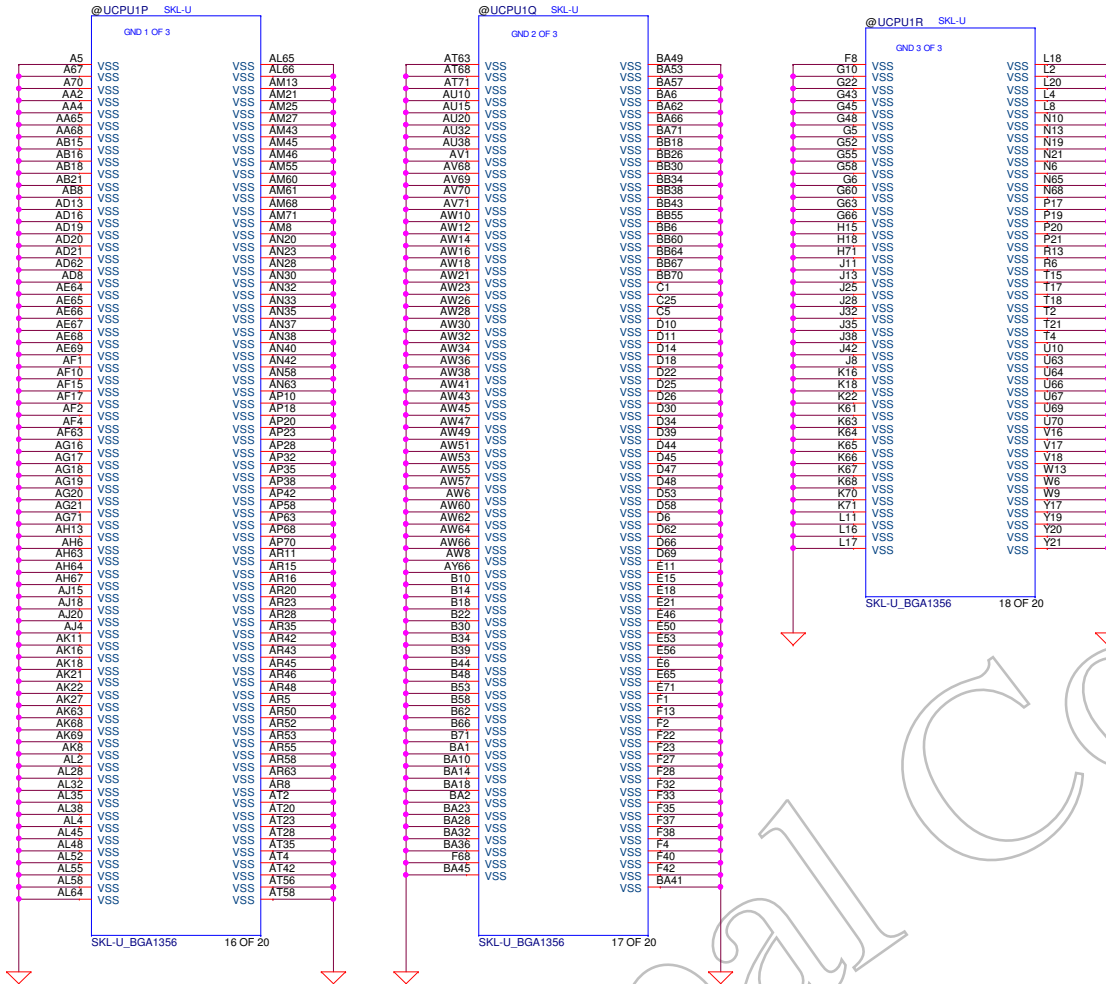
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| Size  | Document Number              | Rev            |
|       | LA-F051P                     | 0.2            |
| Date: | Tuesday, August 01, 2017     | Sheet 18 of 57 |



Take care!!! Note1 on Page 19

Note1: VCCPRIM\_CORE Implementat i on w t h PCH CORE\_V D Reco mnendat i on

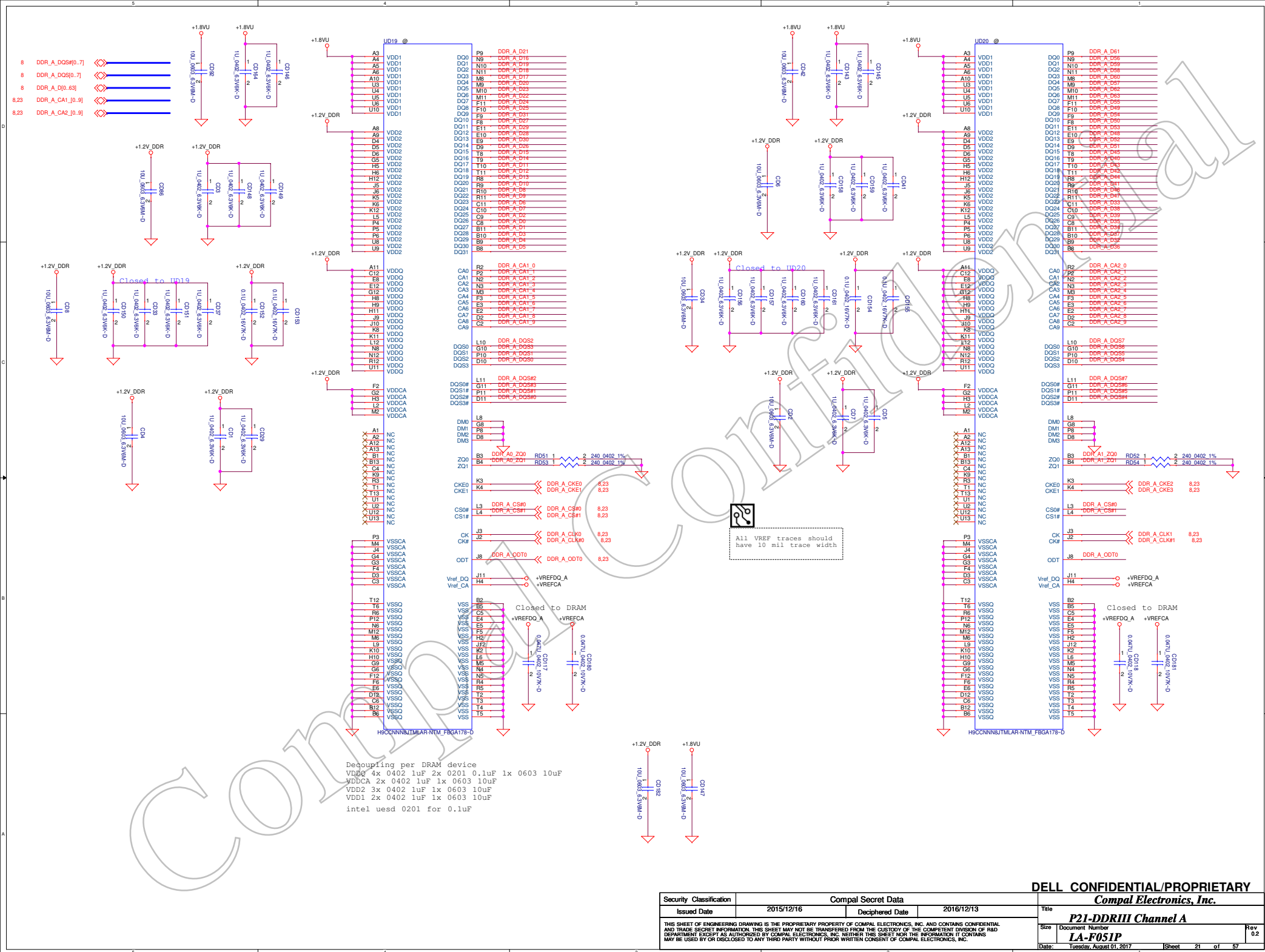
R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



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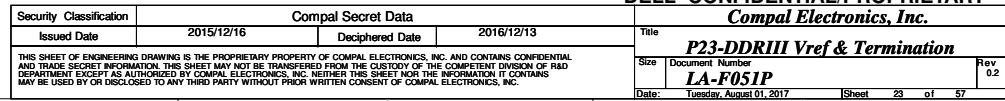
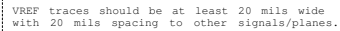
Compal Electronics, Inc.

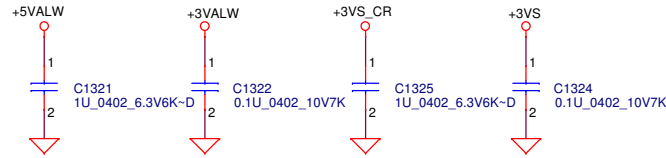
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|   |            |                    |            | Date: Tuesday, August 01, 2017 | Sheet 20 of 57  |



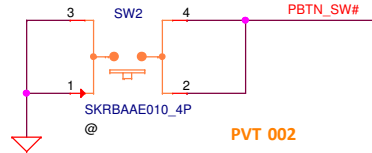








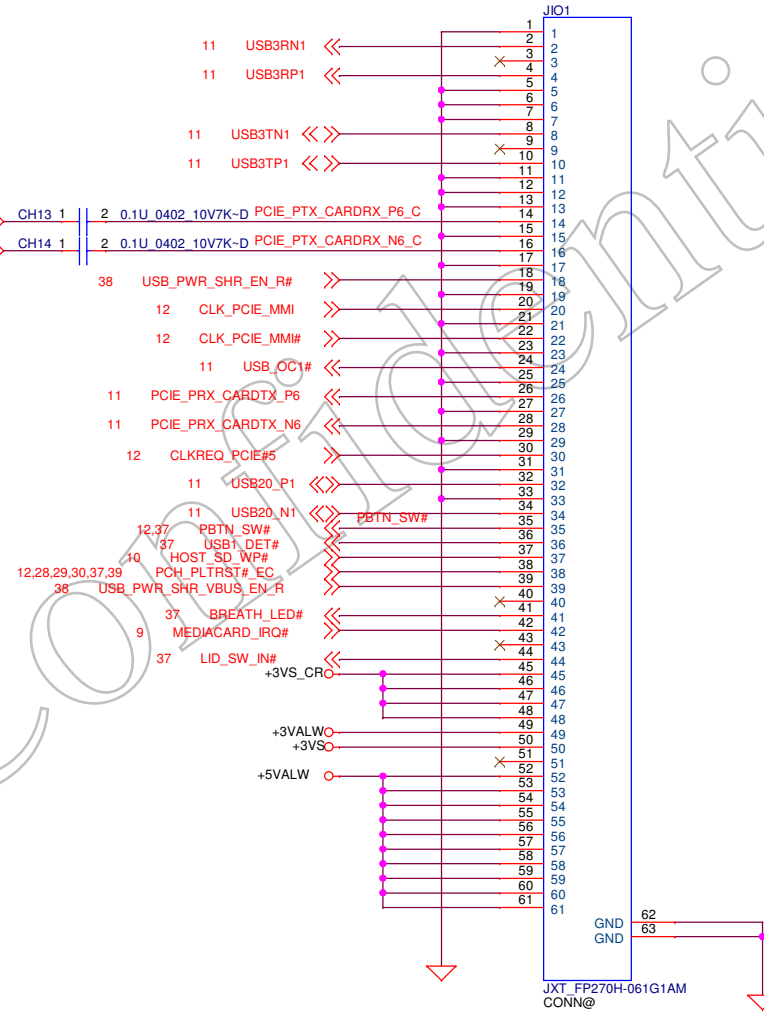
### NPI Stage Power Switch



11 PCIE\_PTX\_CARDRX\_P6  
11 PCIE\_PTX\_CARDRX\_N6

>> CH13 1  
>> CH14 1

2 0.1U 0402 10V7K-D PCIE\_PTX\_CARDRX\_P6\_C  
2 0.1U 0402 10V7K-D PCIE\_PTX\_CARDRX\_N6\_C



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|   |                    |                 |            | Date:           | Tuesday, August 01, 2017 |
|   |                    |                 |            | Sheet           | 24 of 57                 |

Camera + Touch Screen

Camera

Touch Screen

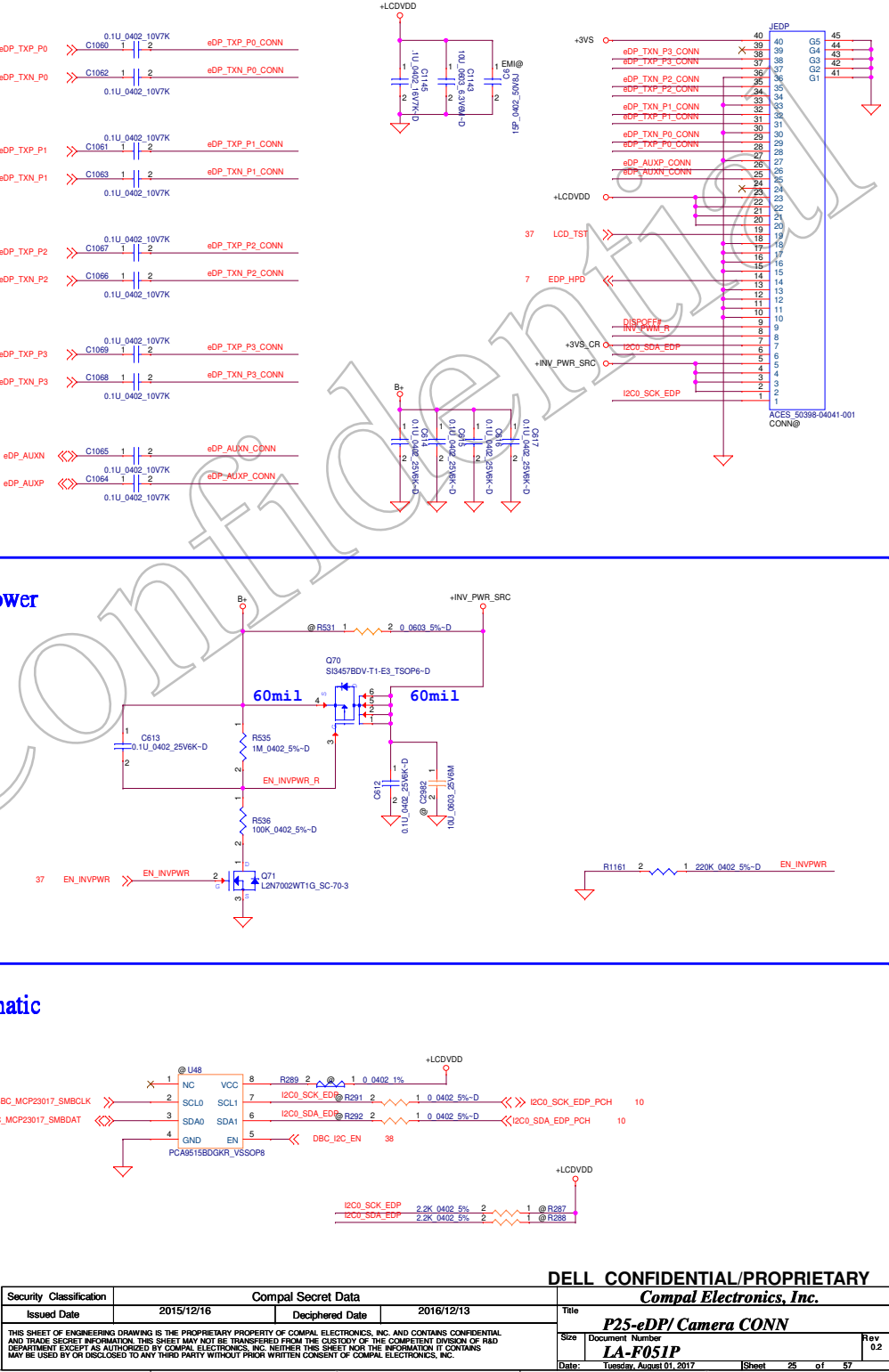
Touch Screen LDO

BackLight PWM Control

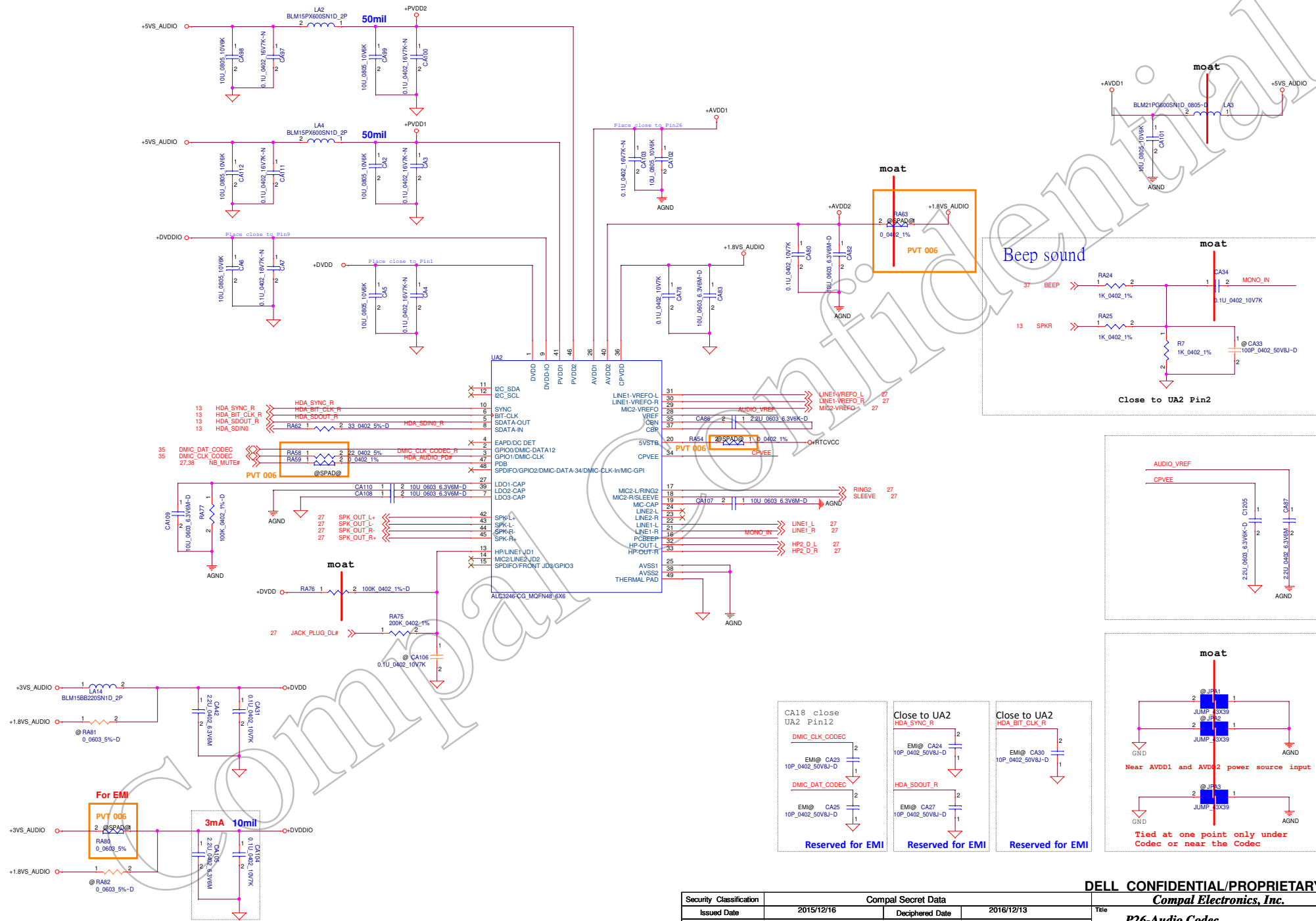
eDP Conn

eDP BackLight Power

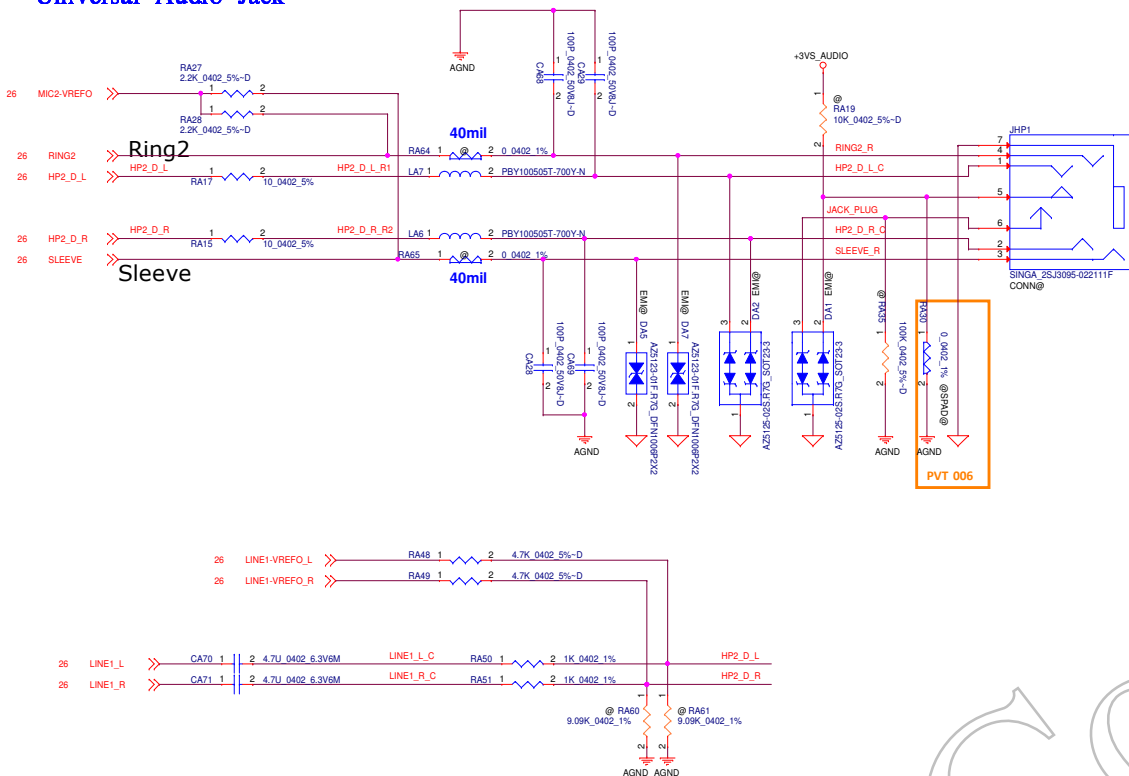
DBC delay schematic



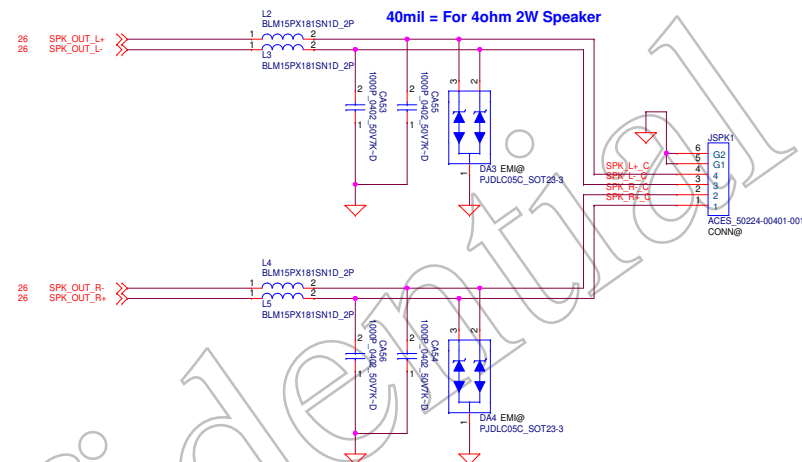
HD Audio Codec



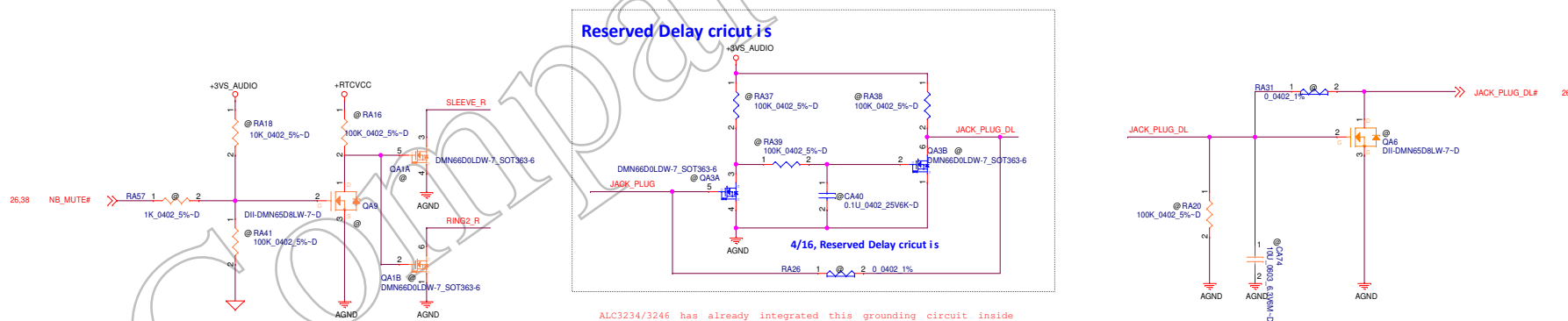
## Universal Audio Jack



Int. Speaker Conn.



## Prevent S3/S4/S5 Background Noise.



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**Compal Electronics, Inc.**

### ***P27-Audio Jack / Speaker***

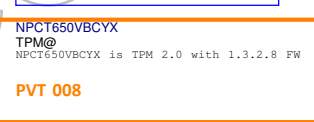
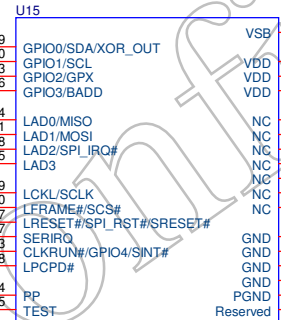
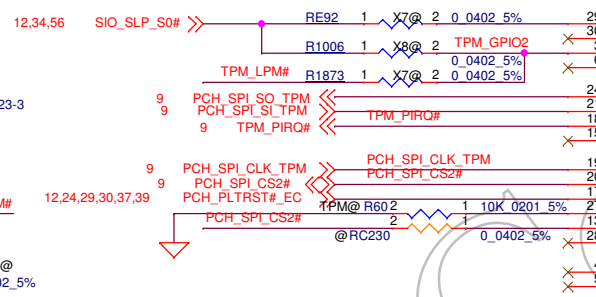
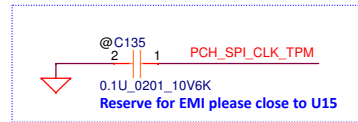
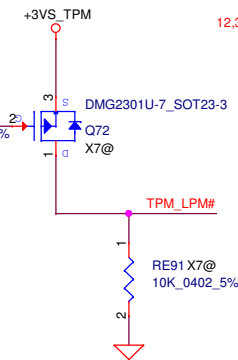
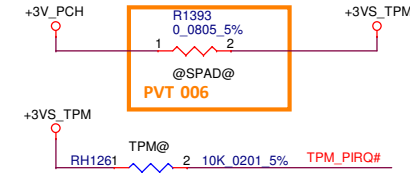
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| Rev | 0.2 |
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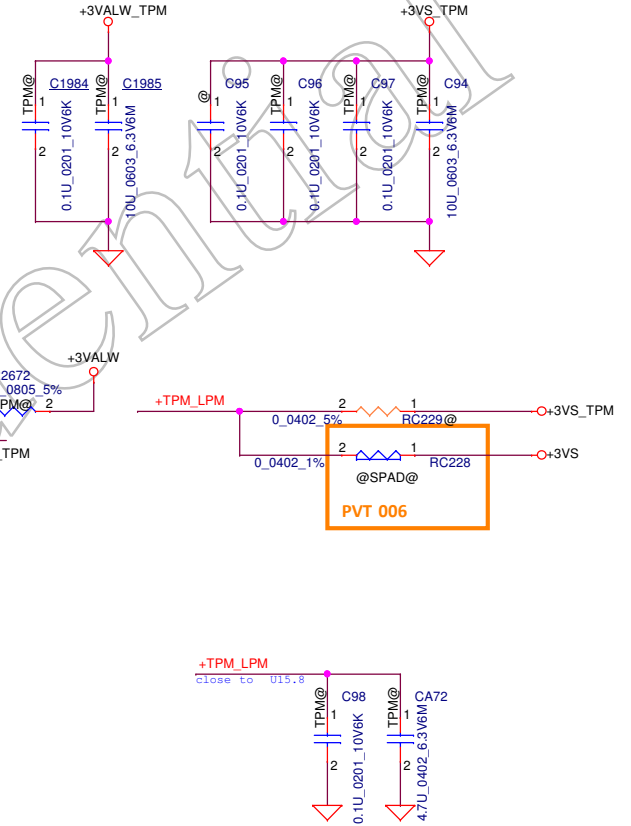
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|-----------|--------------------------|
| LA-T-0511 |                          |
| Date:     | Tuesday, August 01, 2017 |
| Sheet     | 27 of 53                 |

# TPM

NOTE:  
Follow the SPI topology layout guidelines  
in the relevant Intel Platform Design Guide



NOTE:  
Place 0.1 uF capacitors as close as  
possible to the device power pins

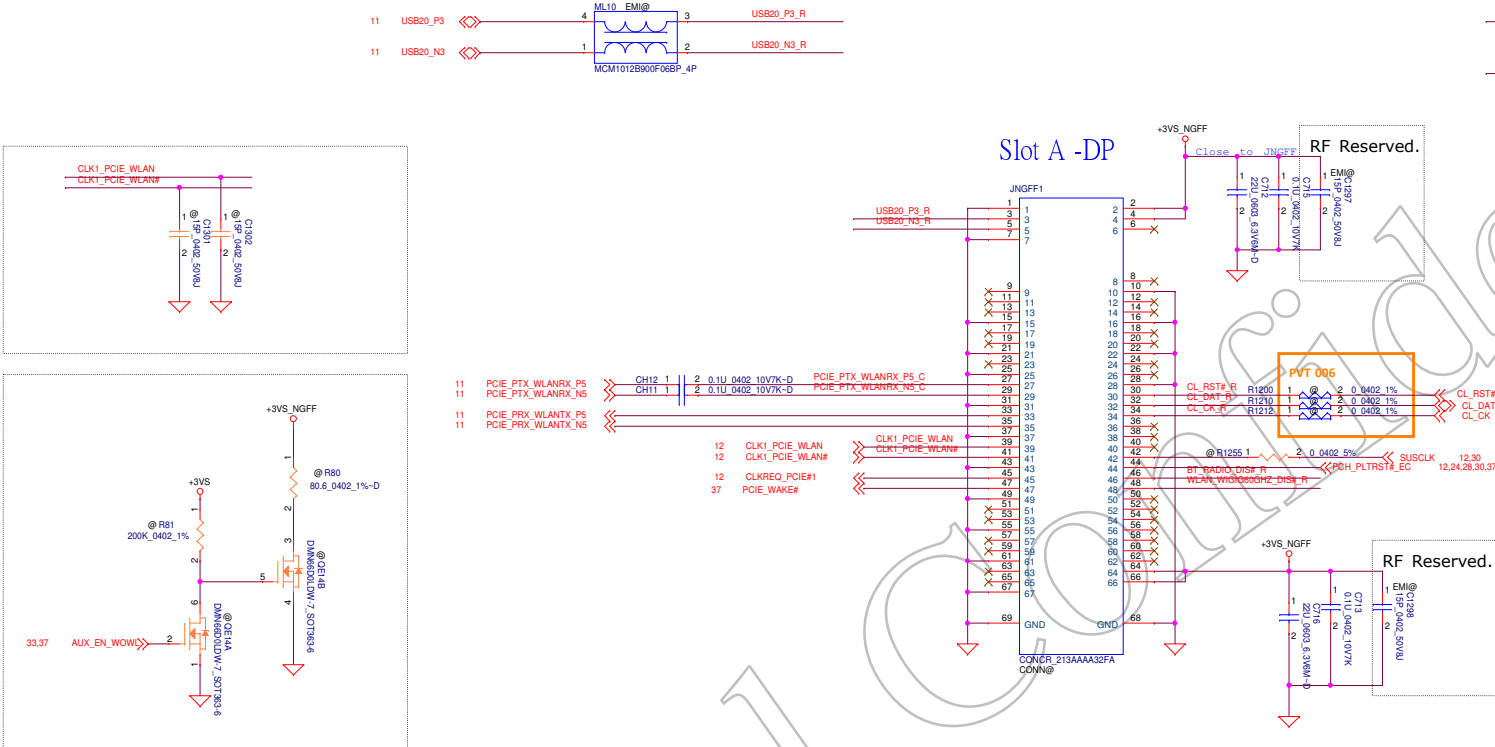


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|   |            |                    |            | LA-F051P | Rev 0.2         |
| Date: Tuesday, August 01, 2017  |            | Sheet 28 of 57     |            |          |                 |

M.2 Slot-A Key-A (WLAN)

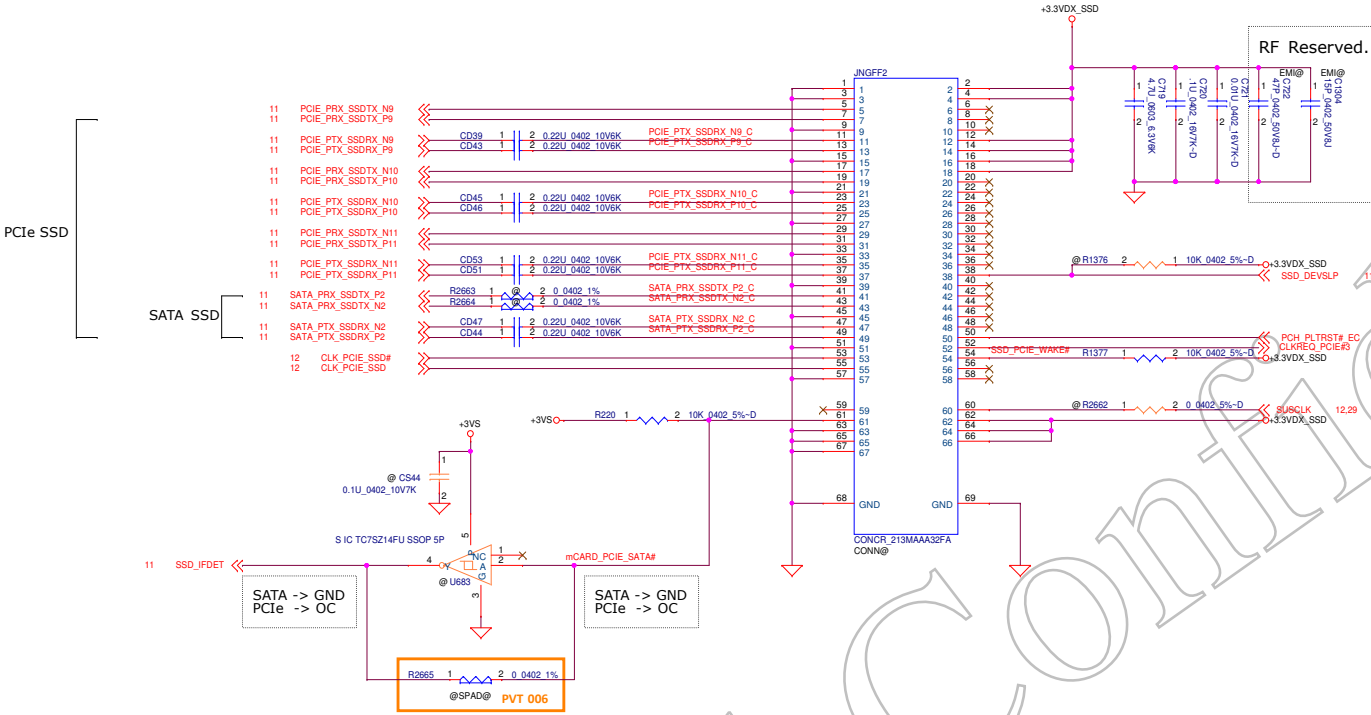


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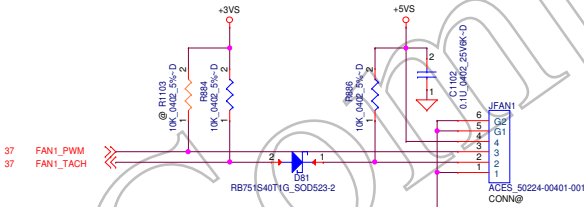
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| Security Classification   | Compal Secret Data | Document Number | LA-F051P                 |
| Issued Date   | 2015/12/16         | Deciphered Date | 2016/12/13               |
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|   |                    | Size            | 29 of 57                 |
|   |                    | Rev             | 0.2                      |
|   |                    | Date            | Tuesday, August 01, 2017 |



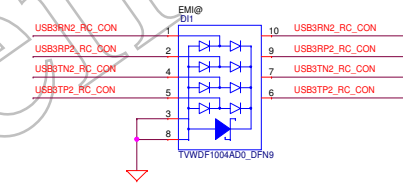
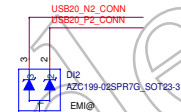
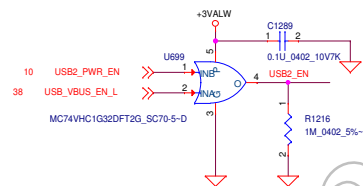
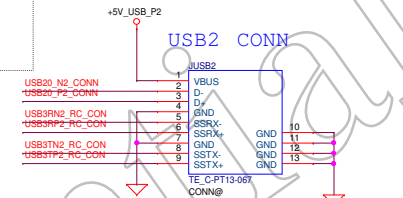
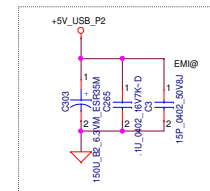
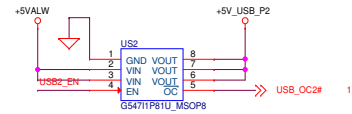
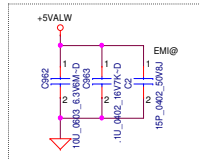
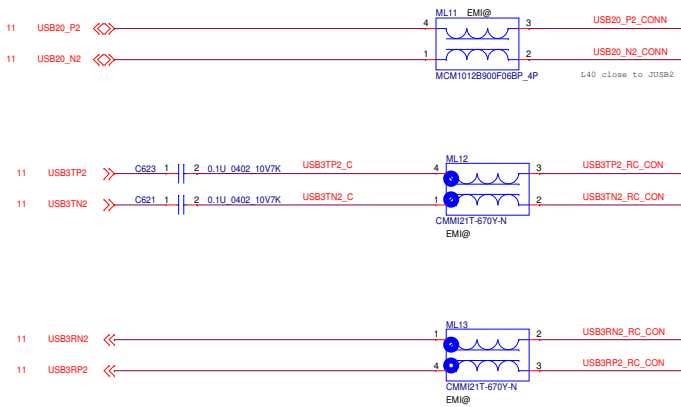
M.2 Slot-C Key-M (SSD)



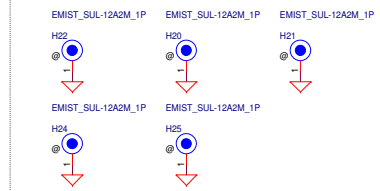
FAN CONN



# USB IO Port



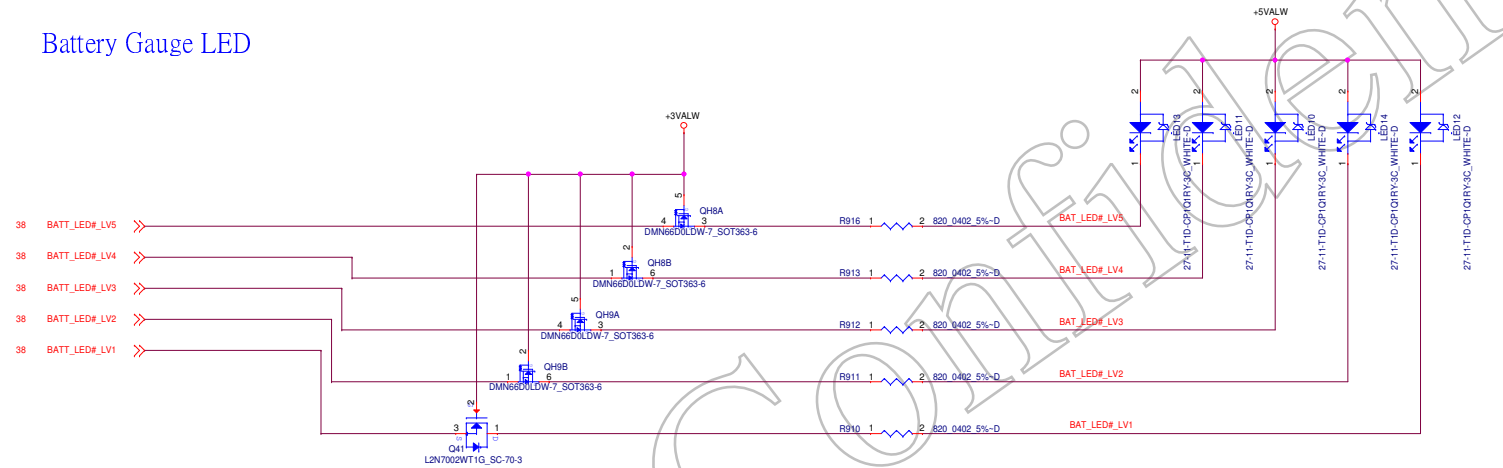
## USB3.0 Shielding Clip



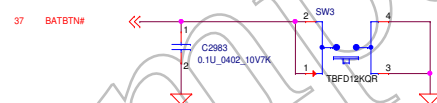
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| Title                   |  |  |  | Document Number          |  |  |  | LA-F051P                      |  |  |  |
| Size                    |  |  |  | Sheet                    |  |  |  | 31 of 57                      |  |  |  |
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# Battery Gauge LED



## Battery Gauge Button

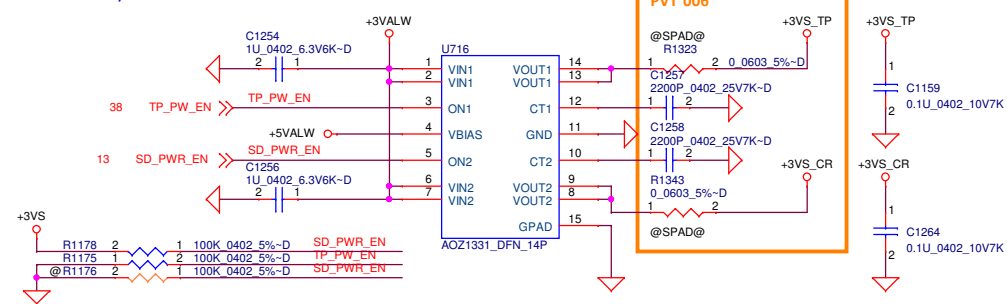


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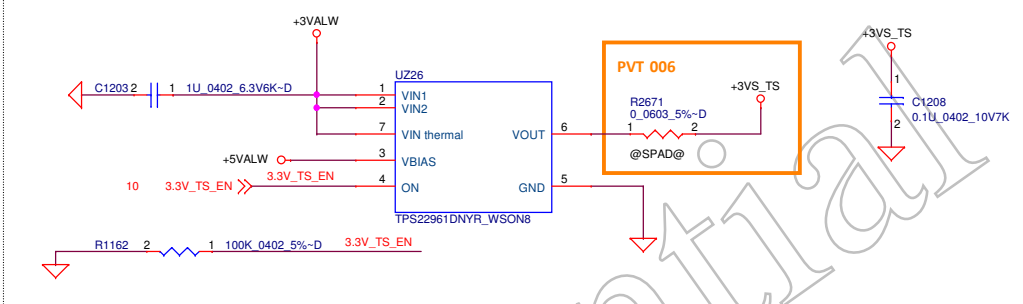
Compal Electronics, Inc.

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|   |                    |                 |            | Document Number                |
|   |                    |                 |            | LA-F051P                       |
|   |                    |                 |            | Rev                            |
|   |                    |                 |            | 0.2                            |
|   |                    |                 |            | Date: Tuesday, August 01, 2017 |
|   |                    |                 |            | Sheet 32 of 57                 |

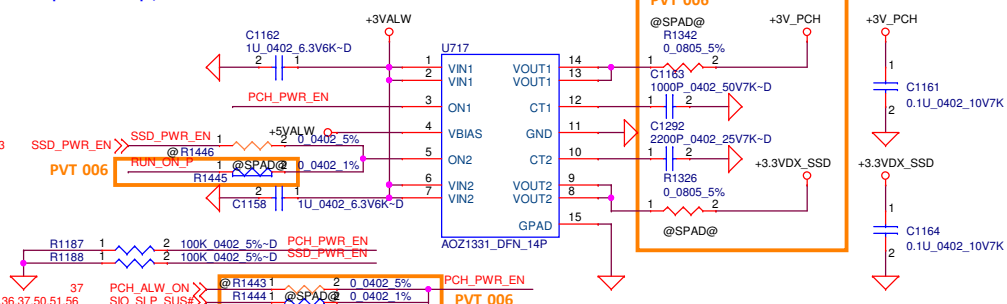
## Touch Pad, Card Reader Load Switch



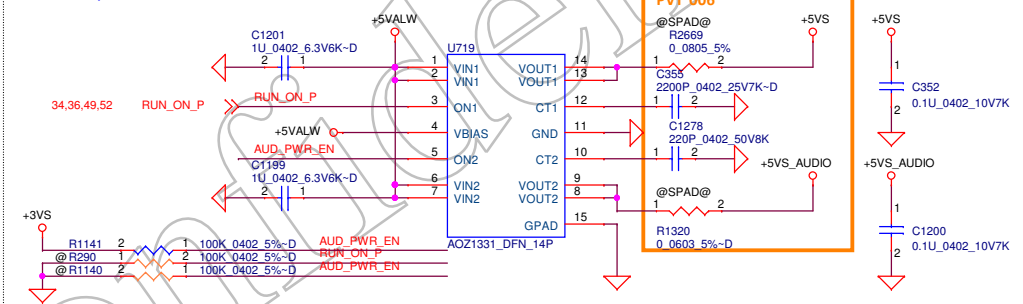
## Touch Screen Load Switch



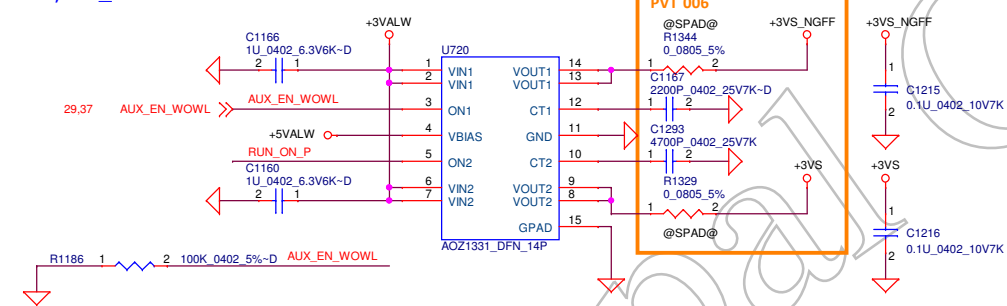
## Deeper Sleep, SSD Load Switch



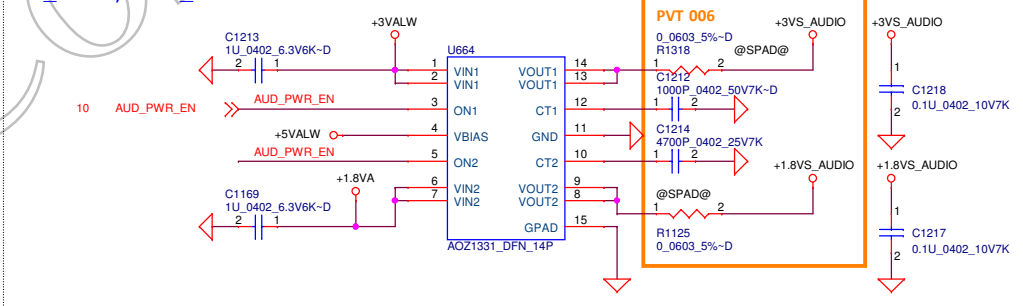
## 5V\_Run, 5V\_Audio Load Switch



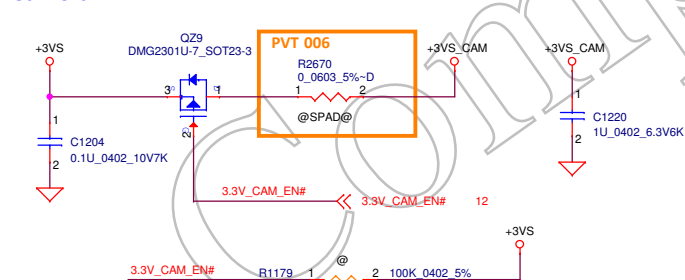
## WiFi, 3V\_RUN Load Switch



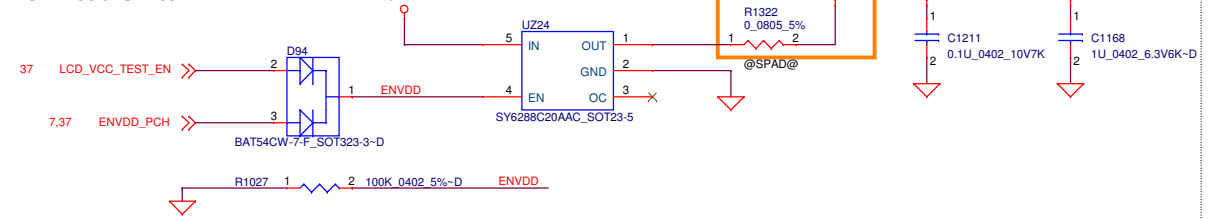
## 3V\_Audio, 1.8V\_Audio Load Switch



## Camera



## LCD Load Switch

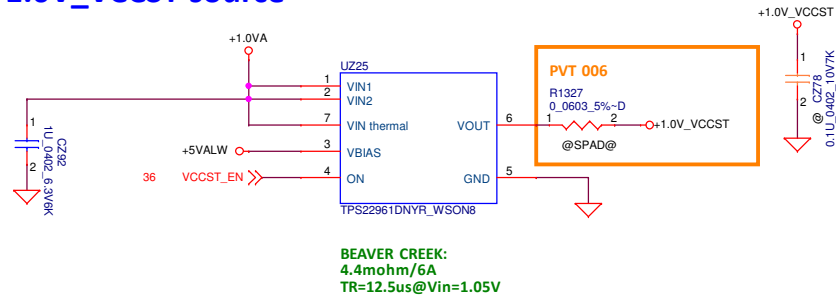


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|                         |  |  |  |                    |  |                 |  | Title                         |  |  |  |
|                         |  |  |  |                    |  |                 |  | P33-DC/DC Interface 1         |  |  |  |
|                         |  |  |  |                    |  |                 |  | Size                          |  |  |  |
|                         |  |  |  |                    |  |                 |  | Document Number               |  |  |  |
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|                         |  |  |  |                    |  |                 |  | Date                          |  |  |  |
|                         |  |  |  |                    |  |                 |  | Tuesday, August 01, 2017      |  |  |  |
|                         |  |  |  |                    |  |                 |  | Sheet                         |  |  |  |
|                         |  |  |  |                    |  |                 |  | 33 of 57                      |  |  |  |

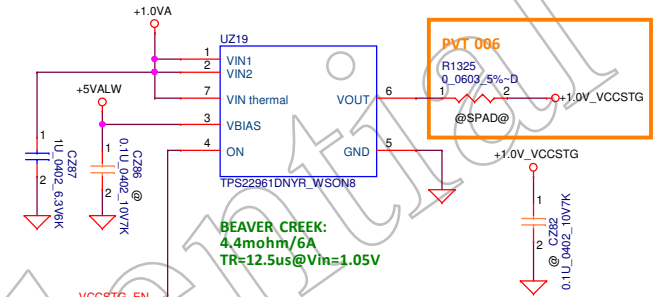
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Size Document Number Rev 0.2

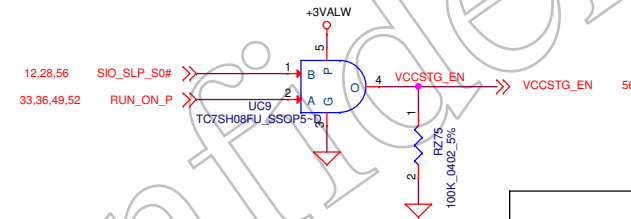
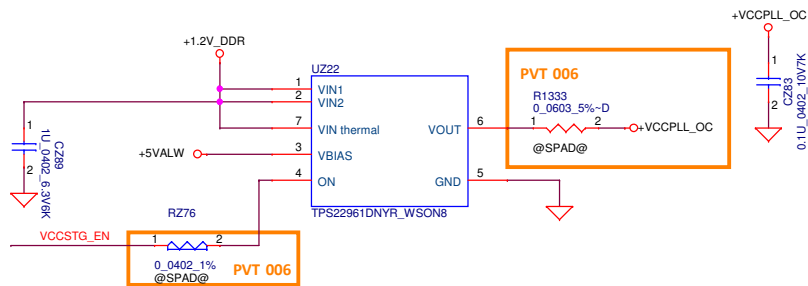
## +1.0V\_VCCST source



## +1.0V\_VCCSTG source

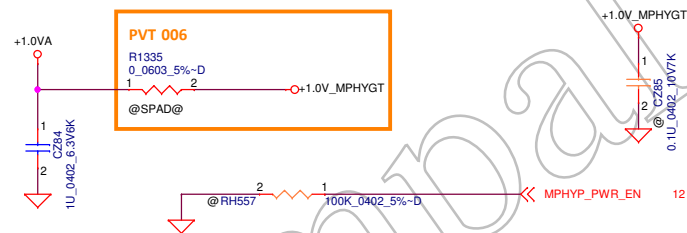


## +VCCPLL\_OC source

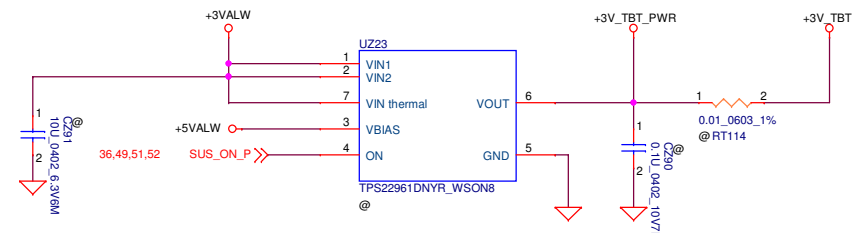


|             | S0   | S0Ix | S3  |
|-------------|------|------|-----|
| SIO_SLP_S0# | high | low  | low |
| RUN_ON_EC   | high | high | low |

## +1.0V\_MPHYGT source

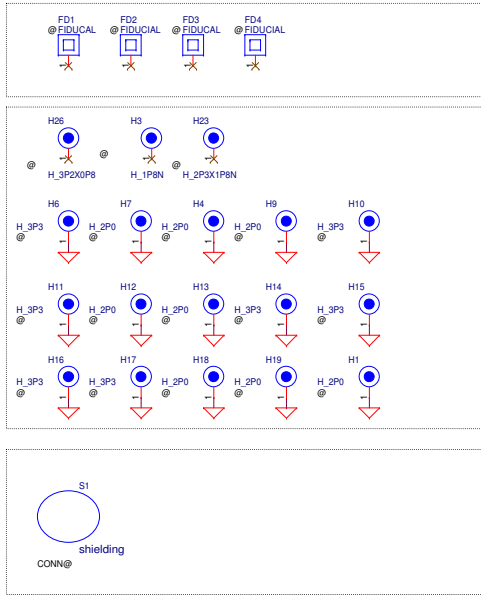


## TBT Power circuits

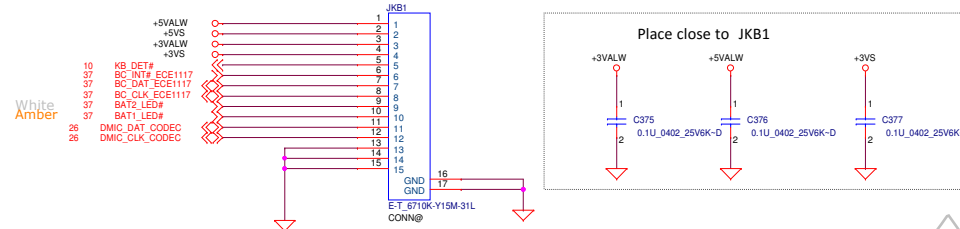


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| Title<br><b>P34-DC/DC Interface 2</b> |                          |                 |          |
| Size                                  | Document                 | Number          | Rev      |
|                                       |                          | <b>LA-F051P</b> | 0.2      |
| Date:                                 | Tuesday, August 01, 2017 | Sheet           | 34 of 57 |

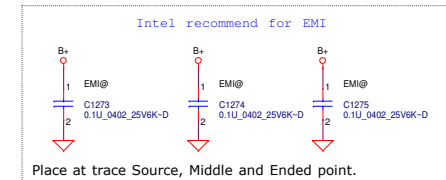
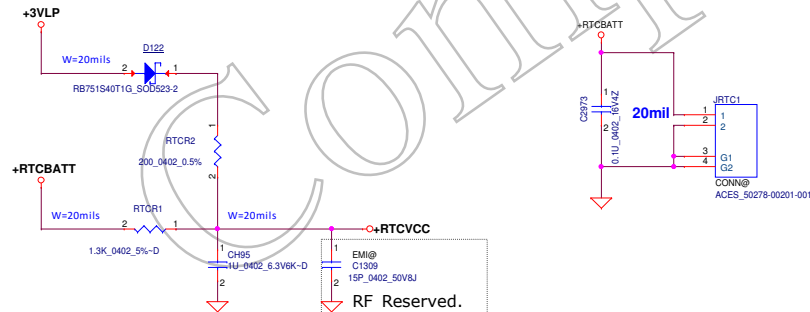


## Keyboard Controller board + DMIC

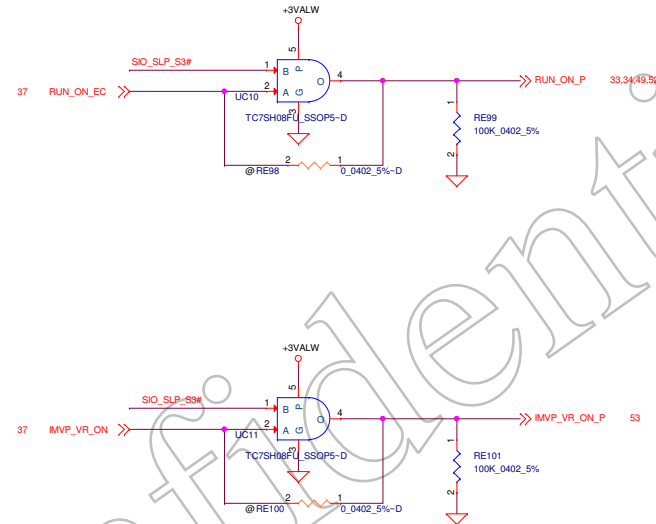
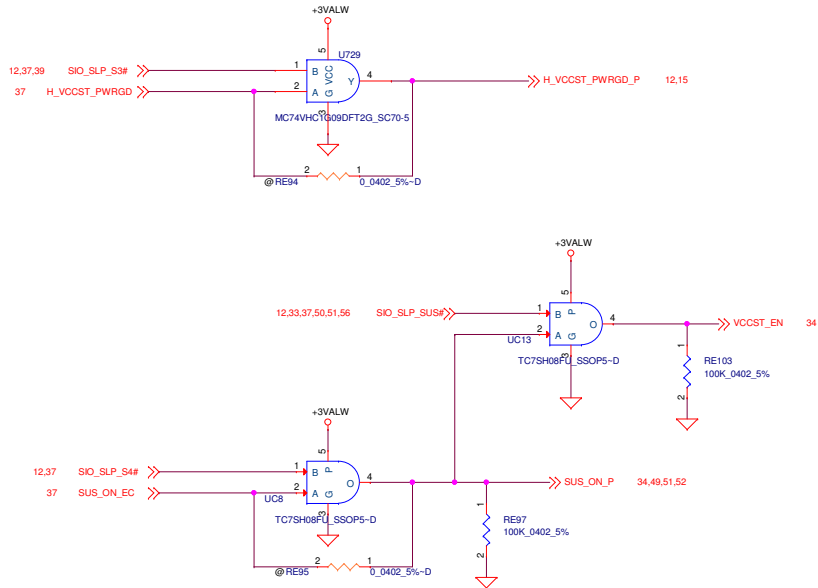


## RTC Battery With Charge Function

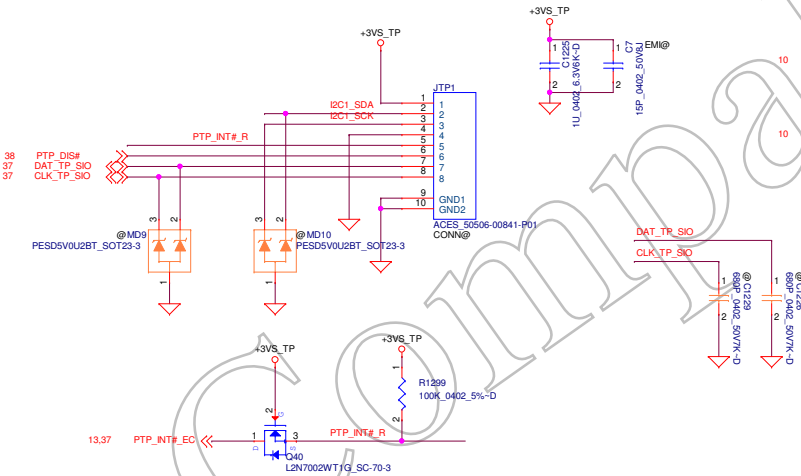
### RTC Battery Conn



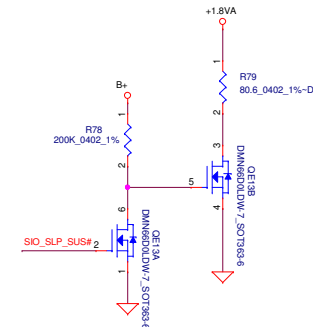
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|   |                    |                 |            | Size                          | Document Number          |
|   |                    |                 |            | LA-F051P                      |                          |
|   |                    |                 |            | Date:                         | Tuesday, August 01, 2017 |
|   |                    |                 |            | Sheet                         | 35 of 57                 |
|   |                    |                 |            | Rev                           | 0.2                      |



## Touchpad CONN



## +1.8VA Discharge

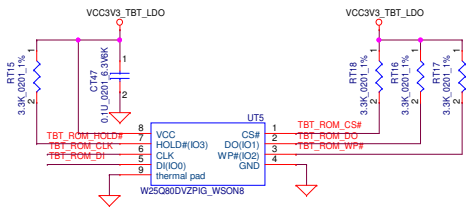
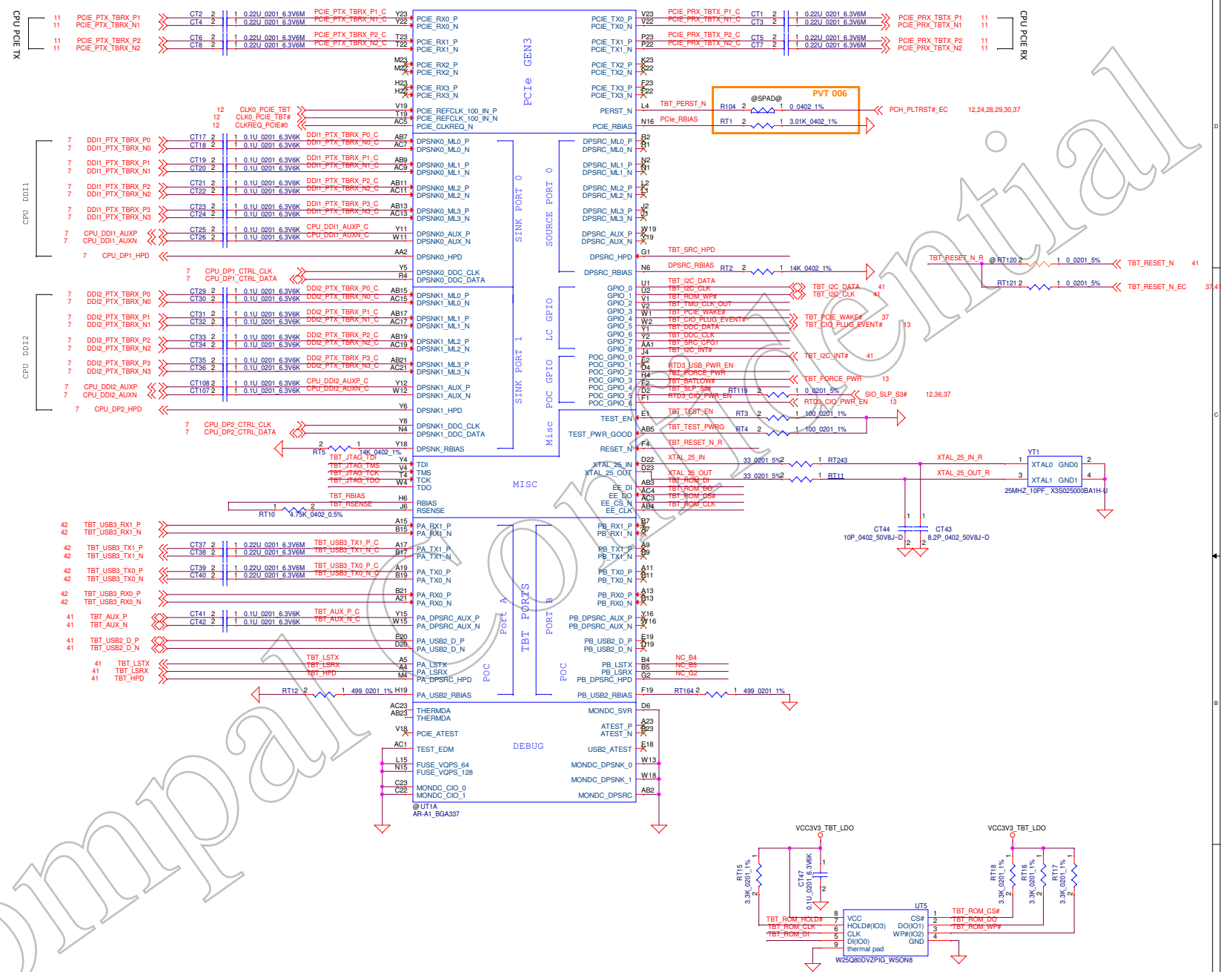
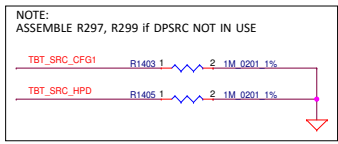
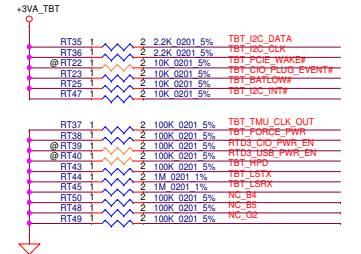
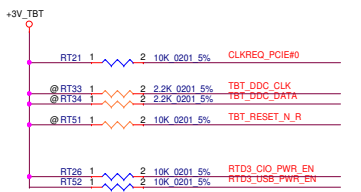
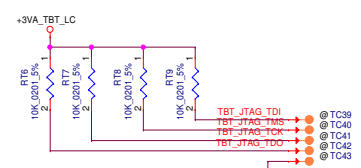


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| P36-TP/PWGRD/LID  |                          | Compal Electronics, Inc.      |            |
| Size  | Document Number          | Rev                           |            |
| LA-F051P  |                          | 0.2                           |            |
| Date:   | Tuesday, August 01, 2017 | Sheet                         | 36 of 57   |



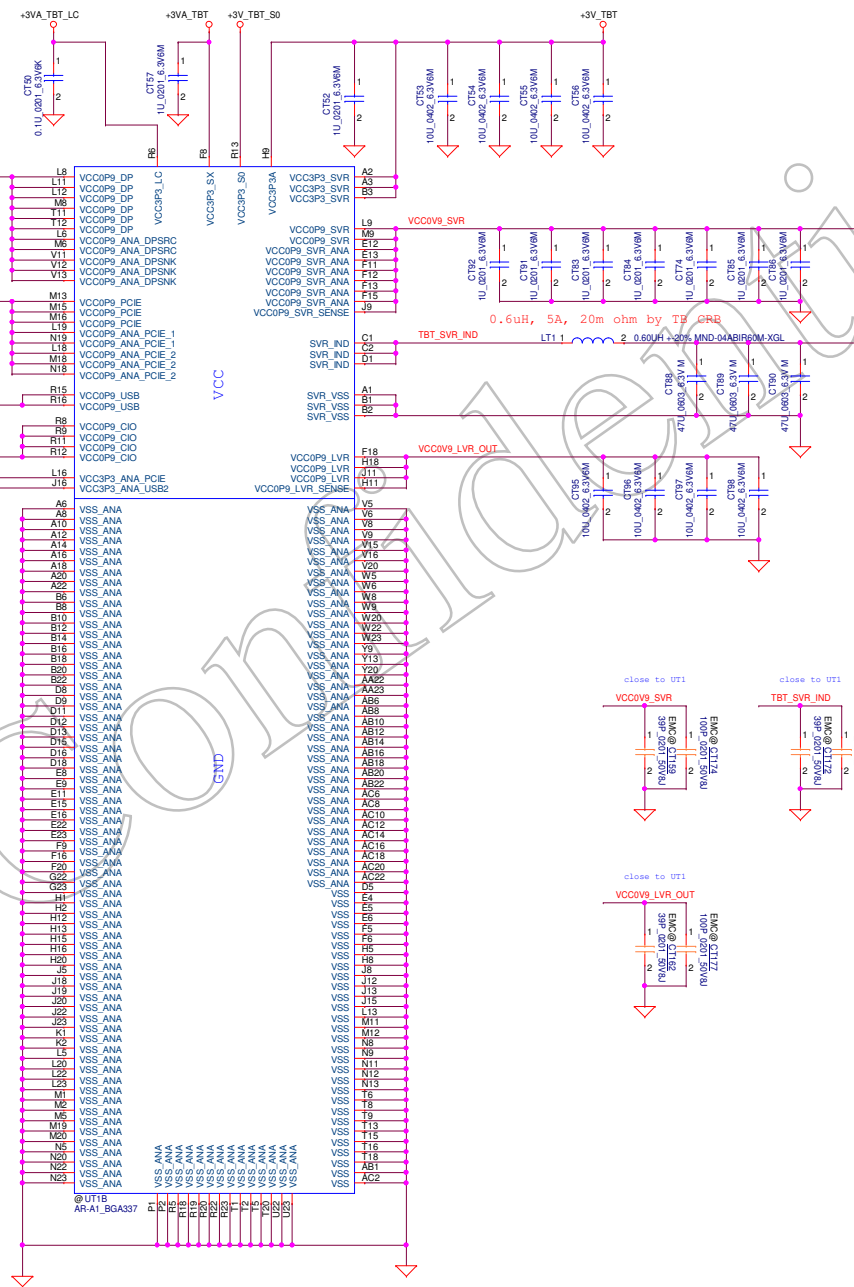
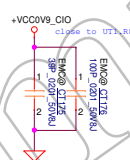
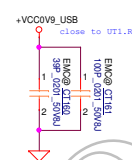
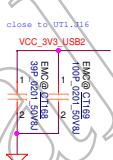
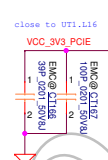
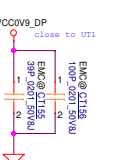
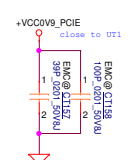
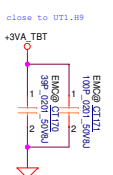
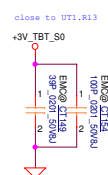
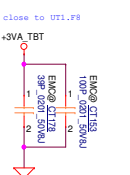
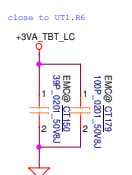
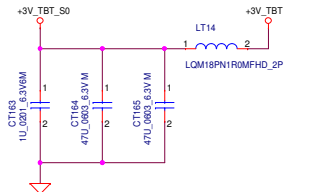
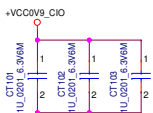
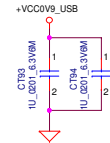
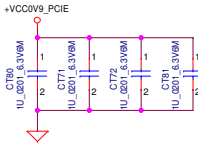
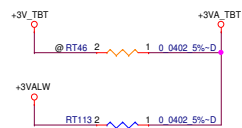
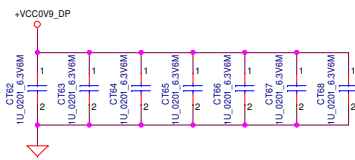






AR/PPS COMMON FLASH

|  |  |                          |  |                               |  |
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| Date:  |  | Tuesday, August 01, 2017 |  | Sheet                         |  |
|  |  |                          |  | 39 of 57                      |  |

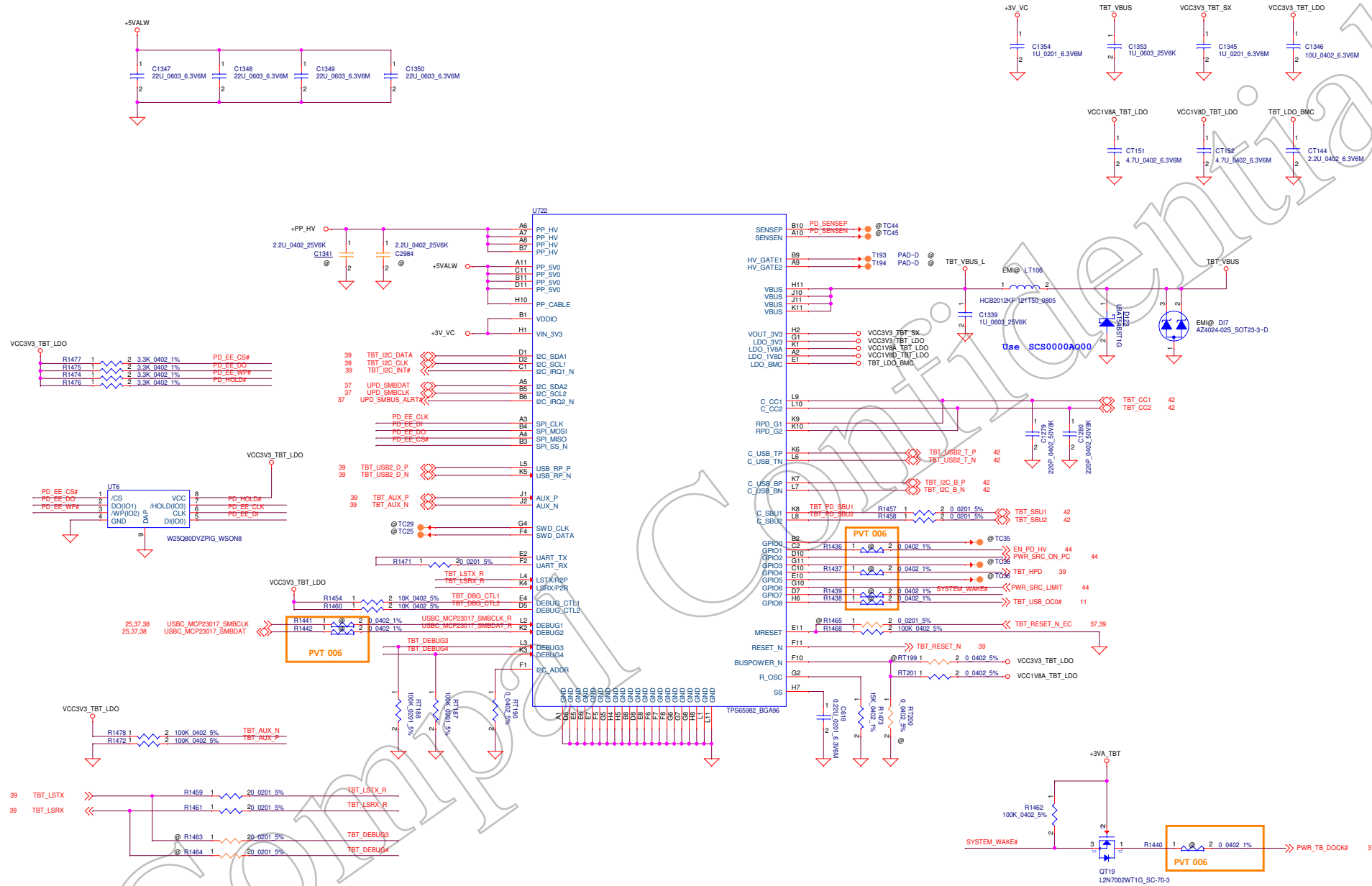


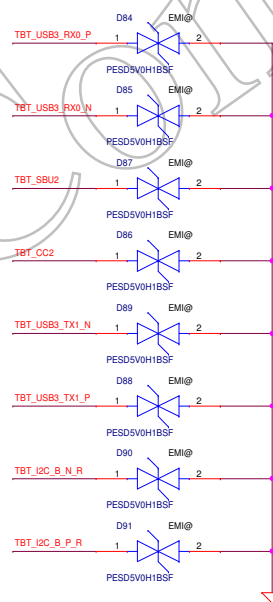
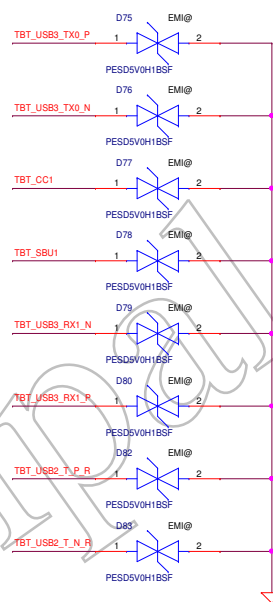
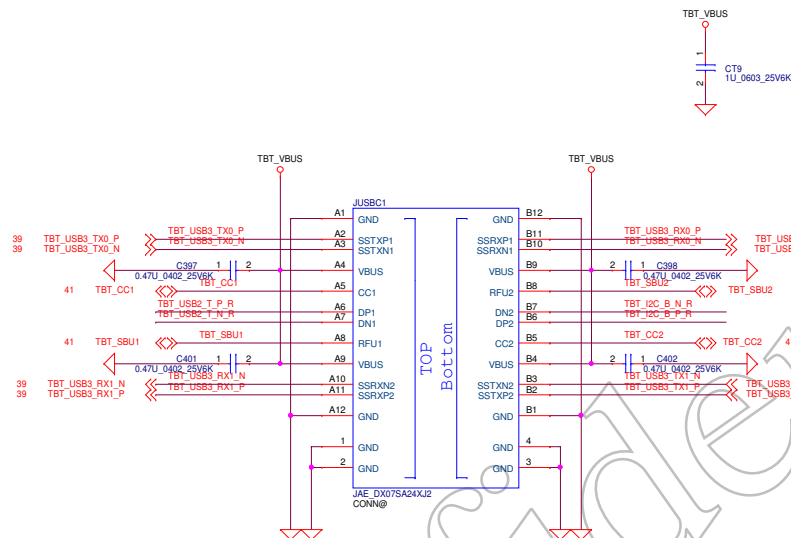
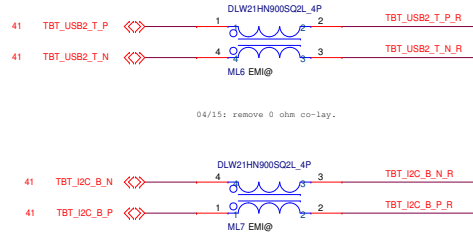
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

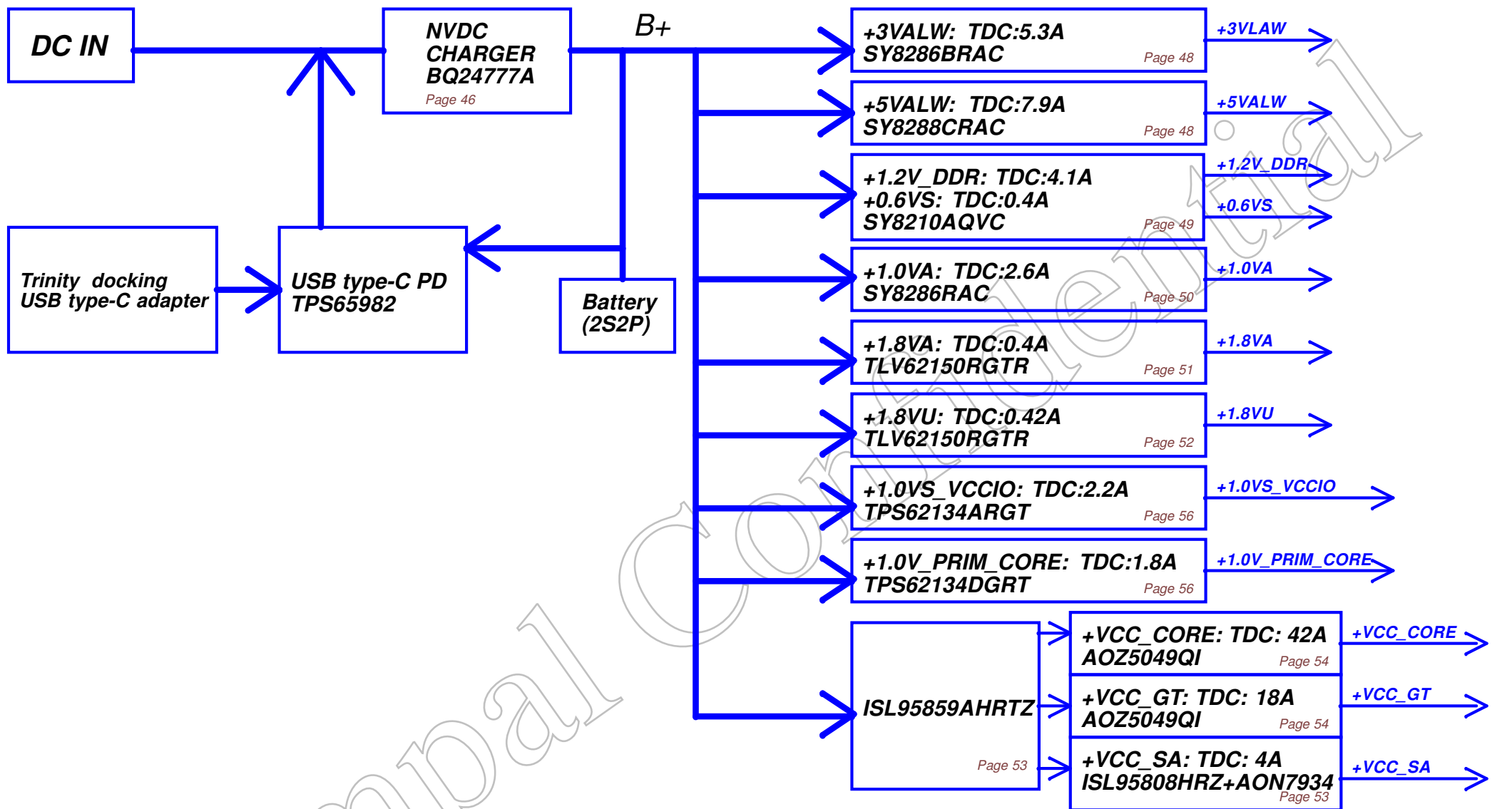
P40-AR TBT (2/2) PWR / VSS

|   |                    |                 |            |
|---|--------------------|-----------------|------------|
| Security Classification   | Compal Secret Data |                 |            |
| Issued Date   | 2015/12/16         | Deciphered Date | 2016/12/13 |
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|   |            |                    |            |                          |                 |
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|   |            |                    |            | Size                     | Document Number |
|   |            |                    |            | LA-F051P                 |                 |
| Date: Tuesday, August 01, 2017  |            | Sheet 43 of 59     |            | Rev 0.1                  |                 |



B+ Power

S8

Barrel Adapter

S1

S2

+SDC\_IN



OCP setting: 3A  
USB type-C PD OCP

USB type-C Adapter

TBT\_VBUS

For Inrush (CTO)

S6  
P-MOSFET

S7  
P-MOSFET

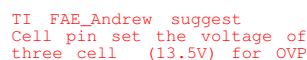
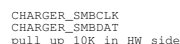
Barrel\_AC Detector

Vbus\_AC Detector

Docking Power Control(41.1), Support component(41.2)

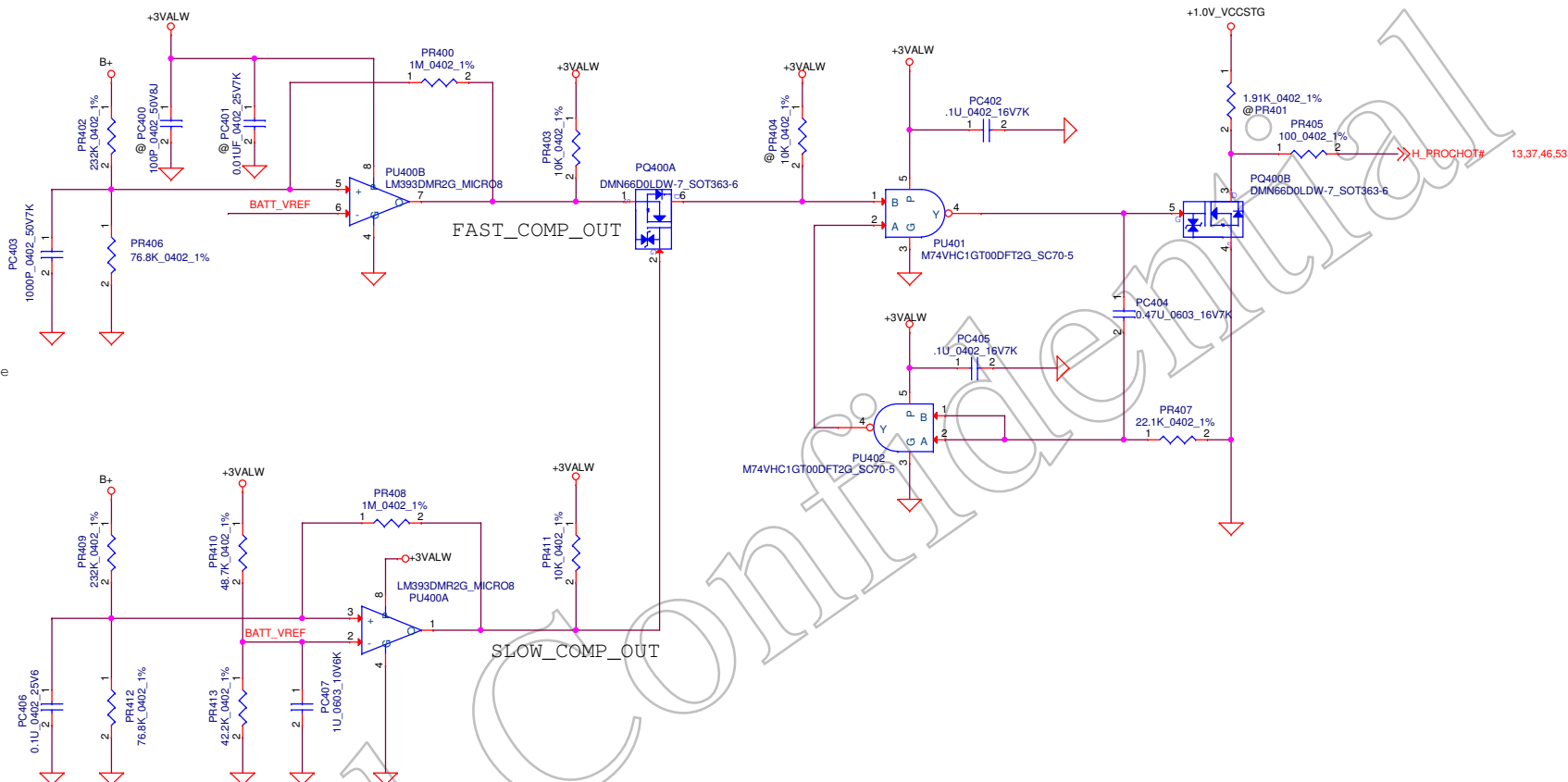
|  |                    |                 |  |
|--|--------------------|-----------------|--|
| Security Classification  | Compul Secret Data |                 | Title  |
| Issued Date  | 2014/10/17         | Deciphered Date | 2014/12/05   |
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|   |                    |                 |            |                          |                 |          |
|---|--------------------|-----------------|------------|--------------------------|-----------------|----------|
| Security Classification   | Compal Secret Data |                 |            | Compal Electronics, Inc. |                 |          |
| Issued Date   | 2014/10/17         | Deciphered Date | 2014/12/05 | Title                    | P46-PWR Charger |          |
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|   |                    |                 |            |                          | LA-F051P        | 0.1      |
| Date:   |                    |                 |            | Tuesday, August 01, 2017 | ISheet          | 46 of 59 |

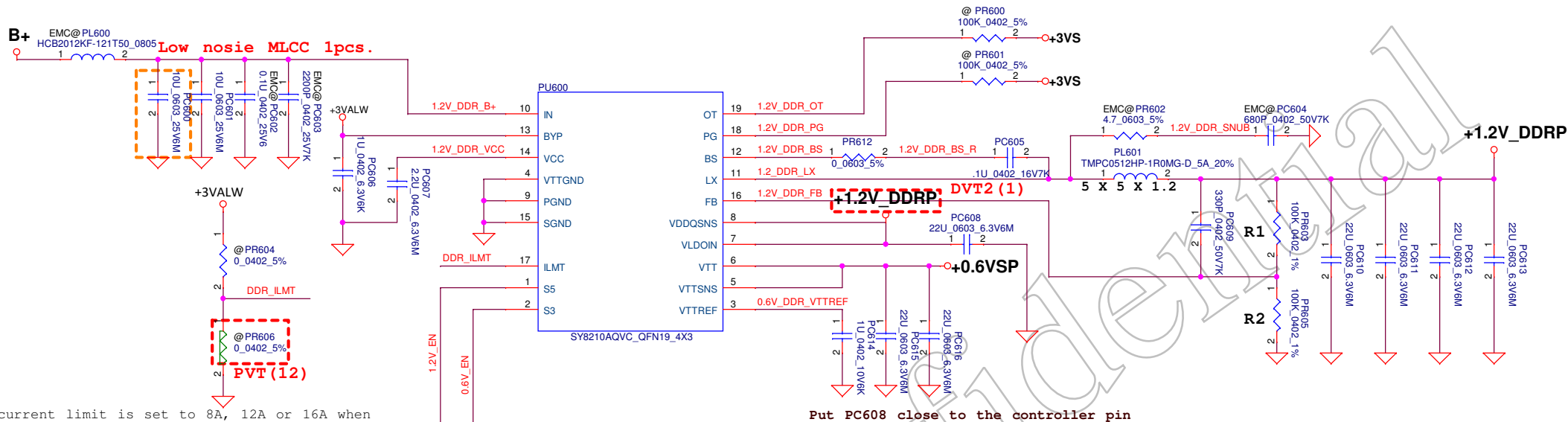
PU400 Main source  
PQ400B open at 3/5V\_B+ below 5.73V  
and 3/5V\_B+ recover 6.05V PQ400B close



Component (37.1)

|   |  |                                 |                 |                          |       |
|---|--|---------------------------------|-----------------|--------------------------|-------|
| Security Classification   |  | Compal Secret Data              |                 | Compal Electronics, Inc. |       |
| Issued Date   |  | 2014/10/17                      | Deciphered Date | 2014/12/05               | Title |
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|   |  | Size                            | Document Number | LA-F051P                 | 0.1   |
| Date:   |  | Tuesday, August 01, 2017        | Sheet           | 47                       | of 59 |





DDR controller(35.3), Support component(35.4)

| Mode     | S3 | S5 | VOUT | VTT |
|----------|----|----|------|-----|
| Normal   | H  | H  | on   | on  |
| Stadby   | L  | H  | on   | off |
| Shutdown | L  | L  | off  | off |

Note: S3 - sleep ; S5 - power off

+1.2V\_DDR  
TDC 4.1A  
Peak Current 5.8A  
OCP Current 8A

0.6Volt +/- 5%  
TDC 0.4A  
Peak Current 0.6A  
OCP Current 2A (fix)

2016/12/06

ADD PR612 0 ohm between PU600 PIN.12 and PC605 PIN.1

| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc. |                         |
|---|------------|--------------------|------------|--------------------------|-------------------------|
| Issued Date   | 2014/10/17 | Deciphered Date    | 2014/12/05 | Title                    | P49-PWR +1.2V DDR/0.6VS |
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|   |            |                    |            | Date                     | LA-F051P                |
|   |            |                    |            | Sheet                    | 49 of 59                |









Local sense put on HW site

+1.0V\_VCCST

PVT (12)

+5VALW

VCC\_SA  
TDC 4A  
Peak Current 6A  
OCP current 10A  
Choke DCR 6.2  $\pm$ 5m ohm

SA\_B+

B+

CPU\_B+

B+

2017/4/17  
Change PC1537 to mount  
on it for noise issue

+VCC\_SA

+3VS

PVT (12)

PVT (13)

PVT (10)

PVT (8)

PVT (2)

PVT (11)

PVT (9)

PVT (1)

PVT (12)

PVT (12)

PVT (12)

PVT (12)

PVT (12)

PVT (12)

PVT (12)

PVT (12)

Local sense put on HW site

VCC\_CORE controller(36.1), Drivers (36.2), Support component(36.3)

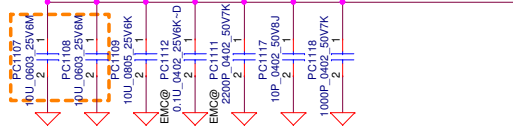
| TYPICAL<br>PROG2<br>RESISTOR<br>( $\pm$ 1%, K $\Omega$ ) | Address<br>Selection | VR A     | VR B     | VR C | VR C<br>Switching<br>Frequency<br>fsw (kHz) |
|--|----------------------|----------|----------|------|---|
| 1.87   | GT [01h]             | IA [00h] | SA [02h] |      | 450   |
| 5.62   | GT [01h]             | IA [00h] | SA [02h] |      | 583   |

| TYPICAL<br>PROG1<br>RESISTOR<br>( $\pm$ 1%, K $\Omega$ ) | VR A and<br>VR B<br>Switching<br>Frequency<br>fsw (kHz) | VR A<br>IA/GT<br>1-Ph<br>(A) | VR B<br>IA/GT<br>1-Ph<br>(A) | VR C<br>GTUS<br>(A) | SA<br>(A) | GTUS<br>(A) |
|--|---|------------------------------|------------------------------|---------------------|-----------|-------------|
| 100  | 750   | 35                           | 40                           | 70                  | 20        | 10          |

| Security Classification   | Compal Secret Data | Title           |
|---|--------------------|-----------------|
| Issued Date   | 2014/10/17         | Deciphered Date |
|   | 2014/12/05         |                 |
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| Date: Tuesday, August 01, 2017  |                    | Sheet 53 of 59  |

CPU\_B+

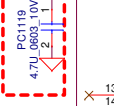
Low nosie MLCC 2pcs.



VCC\_CORE  
TDC 42A  
Peak Current 64A  
OCP current 77A  
Choke DCR 0.9 +-5% ohm

+5VS

PVT (5)



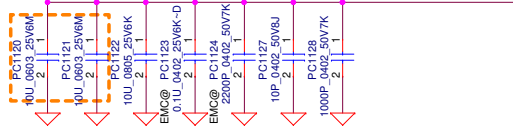
PVT (12)

PVT (4)

PVT (14)

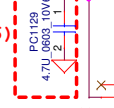
CPU\_B+

Low nosie MLCC 2pcs.



+5VS

PVT (6)



PVT (12)

PVT (4)

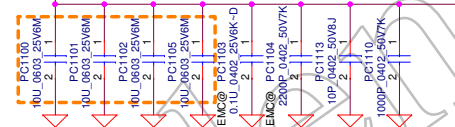
PVT (15)

+VCC\_CORE

+VCC\_CORE

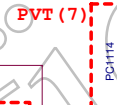
CPU\_B+

Low nosie MLCC 4pcs.



VCC\_GT  
TDC 18A  
Peak Current 31A  
OCP current 37A  
Choke DCR 0.9 +-5% ohm

+5VS



PVT (12)

PVT (4)

PVT (16)

+VCC\_GT

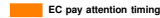
ISUMP\_GT 53 ISUMN\_GT

VCC\_CORE controller(36.1), Drivers (36.2), Support component(36.3)

|   |  |                          |  |                                |  |
|---|--|--------------------------|--|--------------------------------|--|
| Security Classification   |  | Compal Secret Data       |  | Title                          |  |
| Issued Date   |  | Deciphered Date          |  | P54-PWR +VCC CORE/GT ISL95859A |  |
| 2014/10/17  |  | 2014/12/05               |  | Size Document Number           |  |
|   |  |                          |  | LA-F051P                       |  |
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| ITEM | Measure Point         | Time                        |
|------|-----------------------|-----------------------------|
| T1   | +3VALL                | To SLP_SLP_SUS#             |
| T2   | SI0_SLP_SUS#          | To SLP_PCH#                 |
| T3   | SI0_SLP_SUS#          | To +1.8V                    |
| T4   | SI0_SLP_SUS#          | To +1.0V_PRRM_CORE          |
| T5   | SI0_SLP_SUS#          | To +1.0V                    |
| T6   | +3VALL                | To MPPWR_PWR_EN             |
| T7   | MPPWR_PWR_EN          | To +1.0V_MPWRGT             |
| T8   | SI0_SLP_SUS#          | To SUSACK#                  |
| T9   | +1.0V                 | To PCH_RSMRST#              |
| T10  | PCH_RSMRST#           | To AC_PRESENT               |
| T11  | PCH_RSMRST#           | To SLP_SLP_S#               |
| T12  | SI0_SLP_S#            | To SLP_S#                   |
| T13  | SI0_SLP_S#            | To SI0_SLP_WLAN#            |
| T14  | SI0_SLP_WLAN#         | To AUX_EN_WOVL              |
| T15  | AUX_EN_WOVL           | To +3VS_TGFF                |
| T16  | SI0_SLP_S#            | To SLP_SLP_S#               |
| T17  | SI0_SLP_S#            | To +1.0V_VCCST              |
| T18  | SI0_SLP_S#            | To SUS_ON_EG                |
| T19  | SUS_ON_EG             | To +1.8VU                   |
| T20  | SUS_ON_EG             | To +1.8V_DDR                |
| T21  | SI0_SLP_S#            | To SLP_PCH_PWRGD            |
| T22  | SI0_SLP_S#            | To SLP_SLP_S#               |
| T23  | SI0_SLP_S#            | To RUN_ON_EC                |
| T24  | RUN_ON_EC             | To +3.3VDC_SBD              |
| T25  | RUN_ON_EC             | To +1.8V_VCCSTG             |
| T26  | RUN_ON_EC             | To +1.8V_VCCIO              |
| T27  | RUN_ON_EC             | To +3VS                     |
| T28  | RUN_ON_EC             | To +5VS                     |
| T29  | +3VS                  | To RUNPWRK                  |
| T30  | +3VS                  | To MPPWR_PWR_EN             |
| T31  | MPPWR_PWR_EN          | To VCORE_PG (PCH_PWRKOK)    |
| T32  | VCORE_PG (PCH_PWRKOK) | To VCC_SA                   |
| T33  | MPPWR_PWR_EN          | To VLOC_EDRAM               |
| T34  | MPPWR_PWR_EN          | To VLOC_ECPH0               |
| T35  | MPPWR_PWR_EN          | To VLOC_PWRKOK (RESET_OUT#) |
| T36  | PCH_PLURST#           | To VLOC_CORE                |
| T37  | PCH_PLURST#           | To VLOC_GT                  |